EE457: Digital IC Design
Fall Semester 2019
Project 3 Report Cover Sheet

Due 11/13/2019

PROJECT TITLE: 16-to-1 Multiplexer (MUX) Using Both Conventional CMOS and Transmission Gates

Student Name: Kevin Chen

Put Check for completion	Topics	GRADES
✓	Section 1: Executive Summary	/5
✓	Section 2: Introduction and Background	/5
✓	Section 3: Electric Circuit Schematics	/10
✓	Section 4: Detailed Electric Layouts	/25
✓	Section 5: IRSIM Logic Simulations and Measurements for Layout and Schematic (must provide comparisons between the two)	/10
✓	Section 6: LTSPICE code and parasitic extractions with calculation analysis for charge sharing. Put only samples of code.	/15
✓	Section 7: Measurements in LTSPICE for delays for Layout and Schematic (must provide comparisons between the two)	/15
✓	Section 8: Measurements of power, delay, chip area, timing, number of transistors for the layout.	Power /2 Delay /2 Area /2 #tran /4
✓	Section 9: Conclusion and References	/5
	Penalty	
	TOTAL	**/100**

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Section 1: Executive Summary:

In this project, we will be designing a CMOS of a 16-to-1 Multiplexer (MUX) using Electric. By using the Electric software, we'll be creating four different designs, a conventional schematic design, a conventional layout design, a transmission gate (TG) schematic design, and a transmission gate (TG) layout design. The purpose for the use of the transmission gate design is for efficiency and to save on transistors. In order to test if our designs are correct, we'll be generating waveforms to test for correctness by giving a specific input and expecting a certain output. We'll be generating the waveforms using two different software, IRSIM and LTSPICE. The two different software would help support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we'll compare them and observe their similarities and differences.

To design a conventional 16-to-1 Multiplexer (MUX), we plan to use three different designs and combining them together to make a 4-to-1 Multiplexer. One design we plan to use is a three input AND gate, the second design we plan to use is a four input OR gate, and the third design we plan to use is an inverter. By combining four AND gates, one OR gates, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexers and link them together to create a 16-to-1 Multiplexer. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

To design a Transmission Gate (TG) 16-to-1 Multiplexer (MUX), we plan to use two designs and combining them together to make a 4-to-1 Multiplexer. One design we plan to use is an inverter, and the second design we plan to use is a transmission gate. By combining two inverters, and six transmission gates, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexers and link them together to create a 16-to-1 Multiplexer. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

Section 2: Introduction and Background:

A 16-to-1 Multiplexer is a form of digital circuit that is used to select a certain data. The 16-to-1 Multiplexer would have a total of 20 inputs and one output. 16 of the inputs are data, and the other 4 are what's used to select those data. The output would be the one of the 16 inputs, depending on what the selector selects. Multiplexers itself are often used in larger circuitry and helps a lot in terms of which data are being selected so it could be used for modification without modifying the other data. The truth table of the 16-to-1 Multiplexer is shown on Table 1.

The approach we plan to take to design the conventional 16-to-1 Multiplexer would be to use three different designs and combining them together. The three designs that we plan to use would be a three input AND gate, a four input OR gate, and an inverter. The reason for this approach is because we can't directly build a conventional 16-to-1 Multiplexer without first building a 4-to-1 Multiplexer or any Multiplexer, and we can't build a Multiplexer without using an AND gate, OR gate, or an inverter. By applying four AND gates, one OR gate, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexer and link them together to create a 16-to-1 Multiplexer. The figures on the next few pages show the schematic and layout of the two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, an inverter, and a 4-to-1 Multiplexer. In addition, the truth table of a three input AND gate is shown on Table 2; the truth table of a four input OR gate is shown on Table 3; the truth table of an inverter is shown on Table 4; the truth table of a 4-to-1 Multiplexer is shown on Table 5.

The approach we plan to take to design the transmission gate 16-to-1 Multiplexer would be to use two different designs and combining them together. The two designs that we plan to use would be a transmission gate, and an inverter. The reason for this approach is because we can't directly build a transmission gate 16-to-1 Multiplexer without first building a 4-to-1 Multiplexer or any Multiplexer, and we can't build a Multiplexer without using a transmission gate, or an inverter. By applying six transmission gates, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexer and link them together to create a 16-to-1 Multiplexer. The figures on the next few pages show the schematic and layout of the 4-to-1 Multiplexer, which consists of six transmission gates, and two inverters. The truth table of a 4-to-1 Multiplexer is already shown on Table 5.

Table 1: Truth Table of a 16-to-1 Multiplexer

Input: S3	**Input: S2**	**Input: S1**	**Input: S0**	**Output: 16-to-1 Multiplexer**
0	0	0	0	D0
0	0	0	1	D1
0	0	1	0	D2
0	0	1	1	D3
0	1	0	0	D4
0	1	0	1	D5
0	1	1	0	D6
0	1	1	1	D7
1	0	0	0	D8
1	0	0	1	D9
1	0	1	0	D10
1	0	1	1	D11
1	1	0	0	D12
1	1	0	1	D13
1	1	1	0	D14
1	1	1	1	D15

$$Boolean\ Expression:$$

$$Vout = \overline{S_0S_1S_2S_3}D_0 + S_0\overline{S_1S_2S_3}D_1 + \bar{S_0}S_1\overline{S_2S_3}D_2 + S_0S_1\overline{S_2S_3}D_3 + \overline{S_0S_1}S_2\bar{S_3}D_4 + S_0\bar{S_1}S_2\bar{S_3}D_5 + \bar{S_0}S_1S_2\bar{S_3}D_6 + S_0S_1S_2\bar{S_3}D_7 + \overline{S_0S_1S_2}S_3D_8 + S_0\overline{S_1S_2}S_3D_9 + \bar{S_0}S_1\bar{S_2}S_3D_{10} + S_0S_1\bar{S_2}S_3D_{11} + \overline{S_0S_1}S_2S_3D_{12} + S_0\bar{S_1}S_2S_3D_{13} + \bar{S_0}S_1S_2S_3D_{14} + S_0S_1S_2S_3D_{15}$$

Table 2: Truth Table of a Three Input AND Gate

Input: A	**Input: B**	**Input: C**	**Output: A AND B AND C**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$$Boolean\ Expression:$$
$$Vout = A * B * C$$

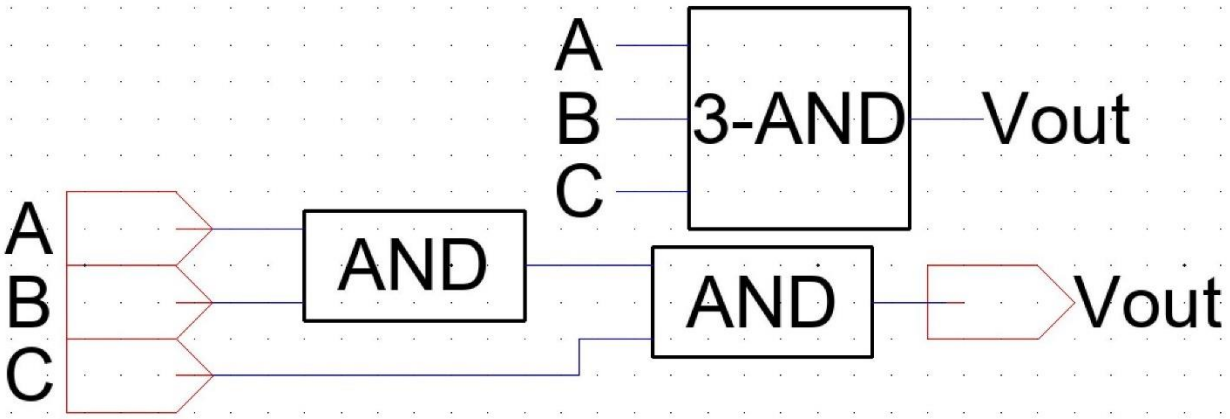

Figure 1: Schematic Design of a Three Input AND Gate

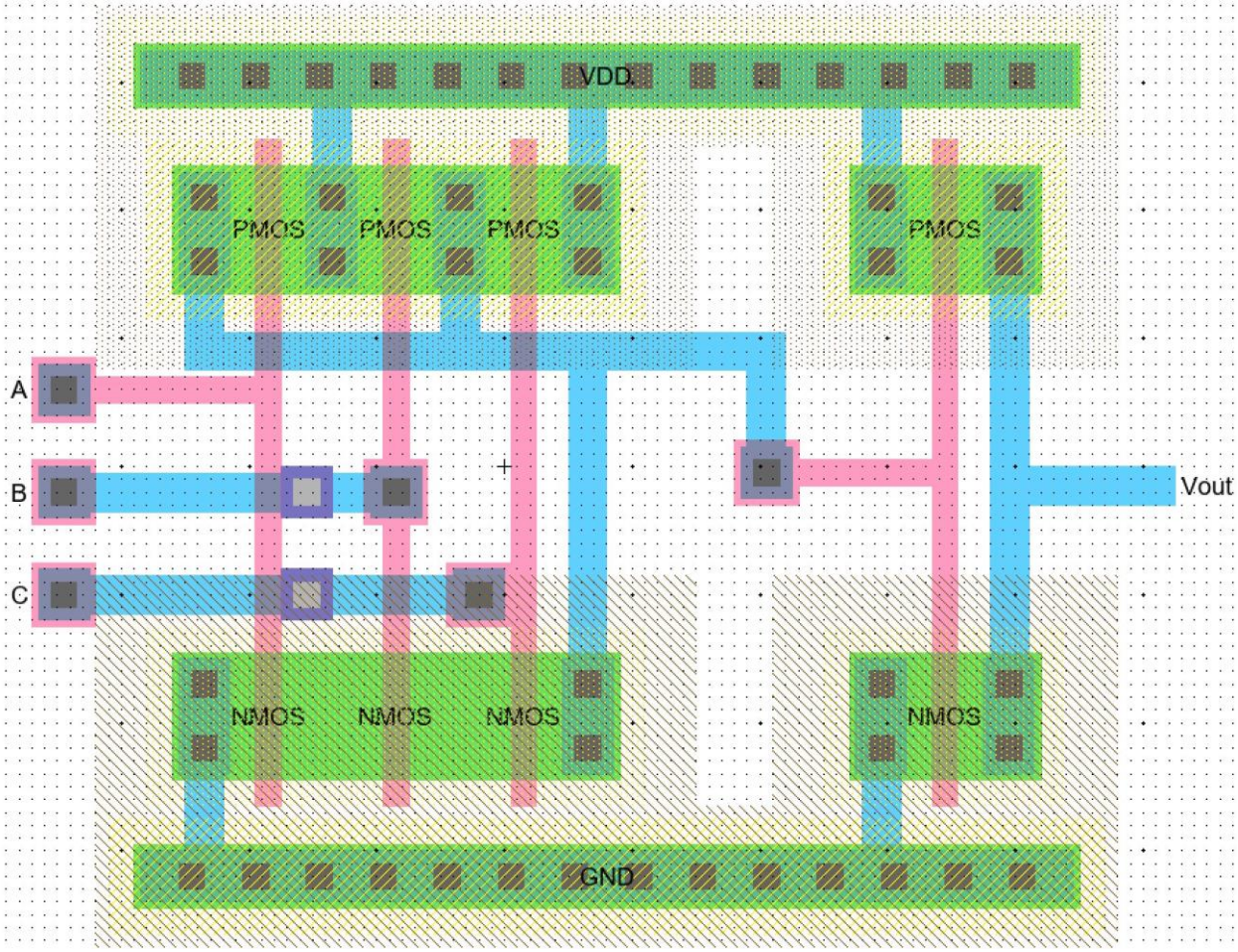

Figure 2: Layout Design of a Three Input AND Gate

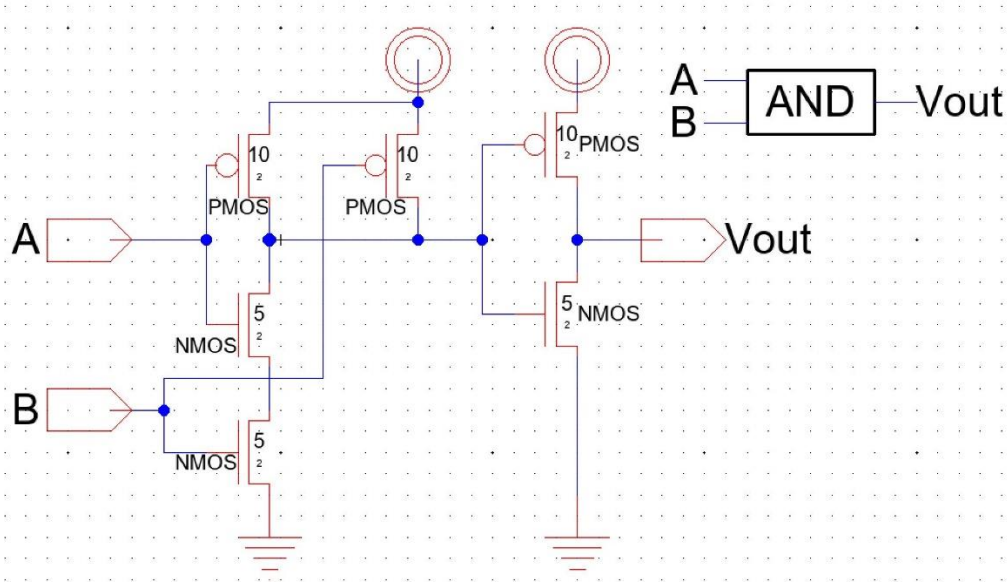

Figure 3: Schematic Design of a Two Input AND Gate That's Used

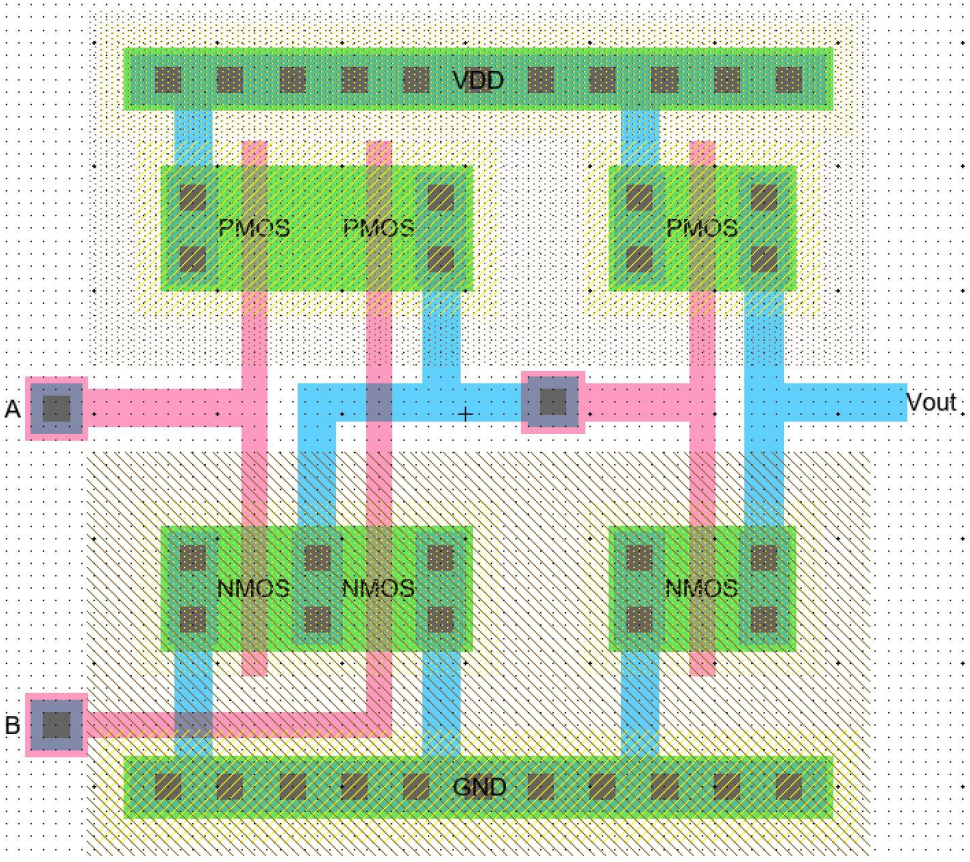

Figure 4: Layout Design of a Two Input AND Gate That's Used

Table 3: Truth Table of a Four Input OR Gate

Input: A	**Input: B**	**Input: C**	**Input: D**	**Output: A OR B OR C OR D**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$$Boolean\ Expression:$$
$$Vout = A + B + C + D$$

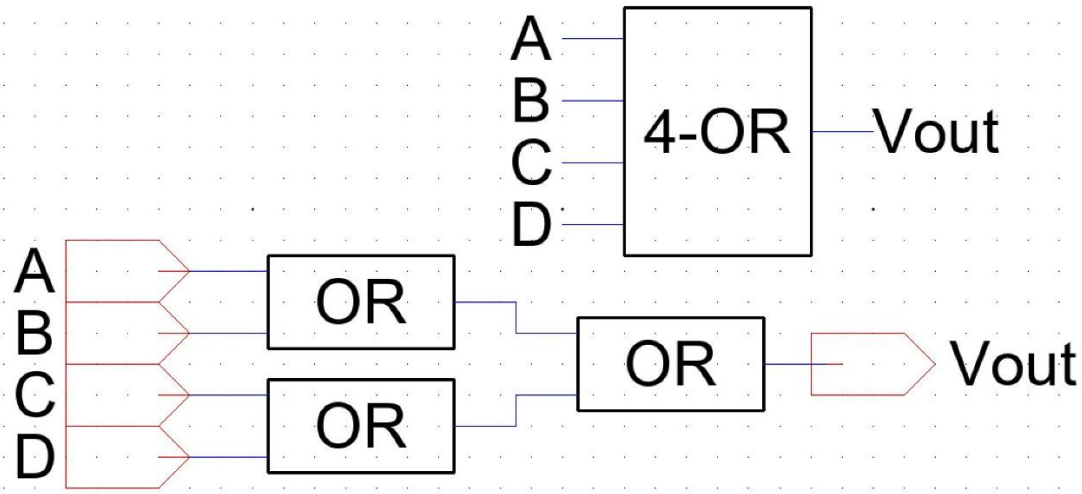

Figure 5: Schematic Design of a Four Input OR Gate

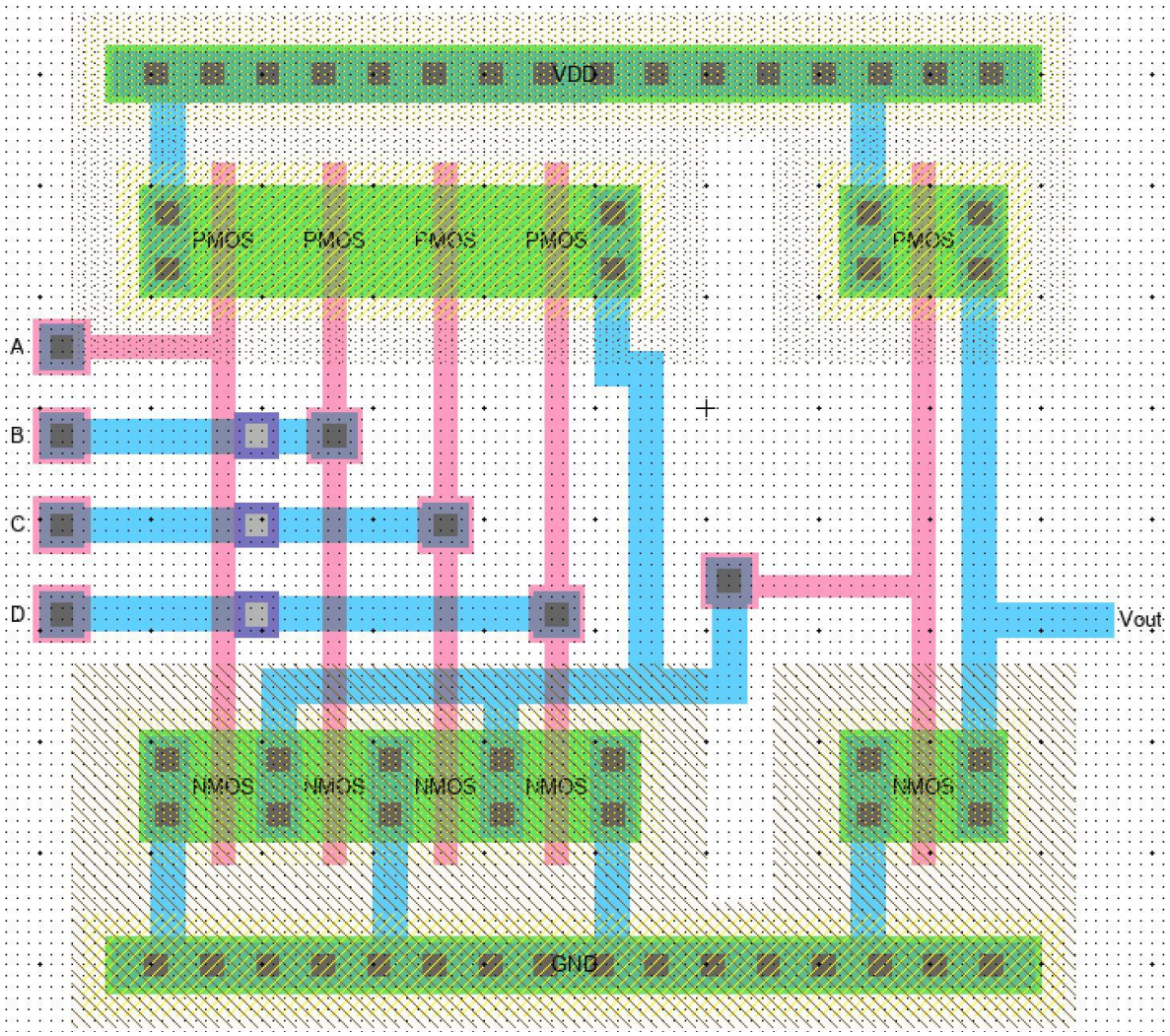

Figure 6: Layout Design of a Four Input OR Gate

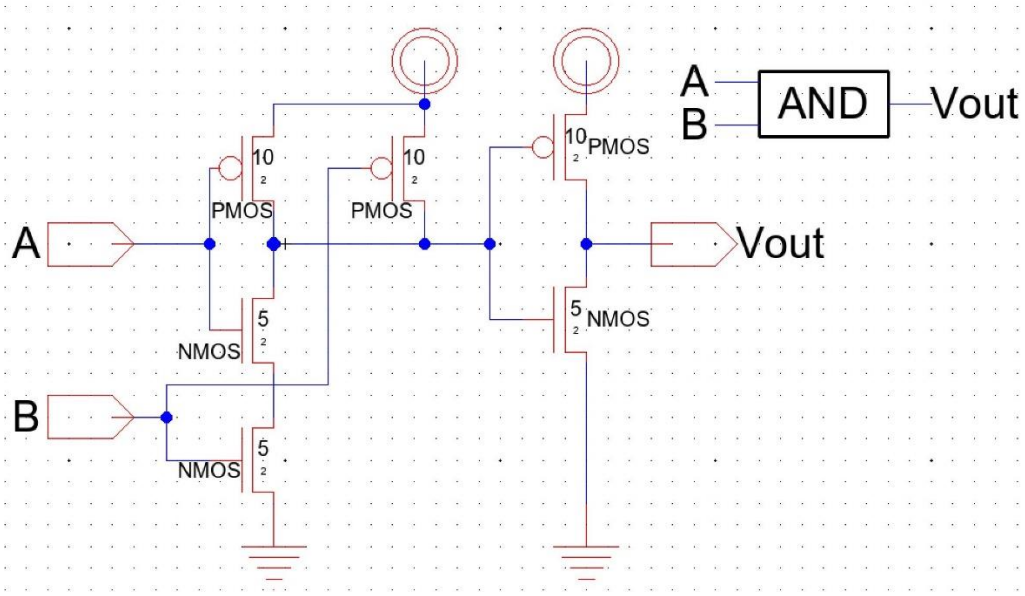

Figure 7: Schematic Design of a Two Input OR Gate That's Used

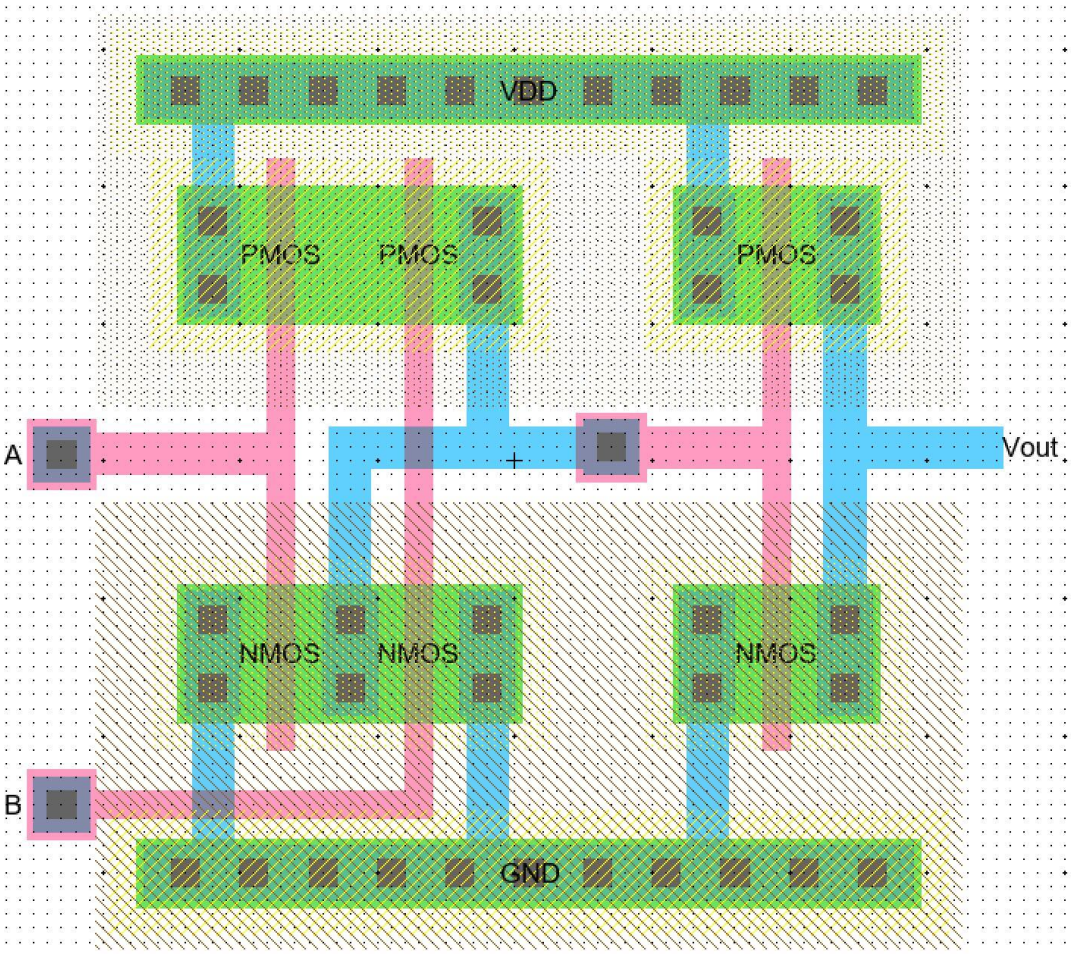

Figure 8: Layout Design of a Two Input AND Gate That's Used

Table 4: Truth Table of an Inverter

Input: In	Output: In NOT
0	1
1	0

$Boolean\ Expression$:

$Vout = \overline{In}$

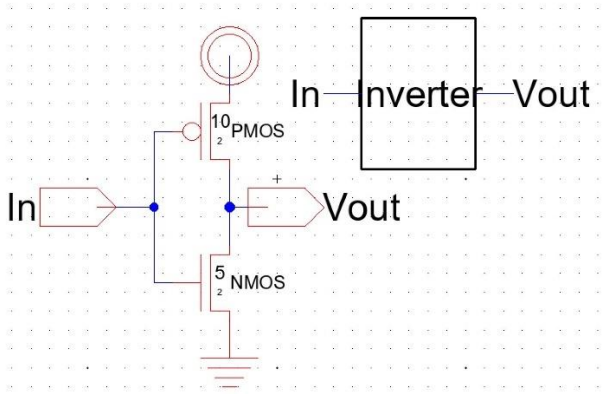

Figure 9: Schematic Design of an Inverter

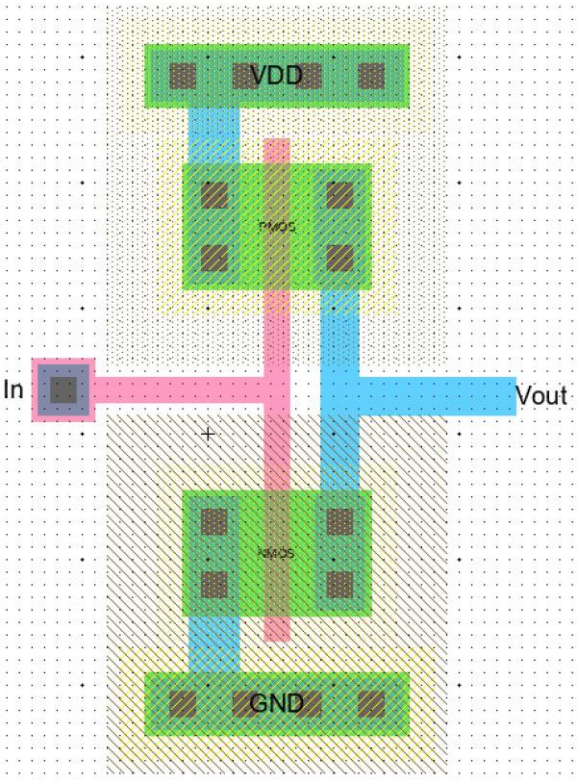

Figure 10: Layout Design of an Inverter

Table 5: Truth Table of a 4-to-1 Multiplexer

Input: S1	Input: S0	Output: 4-to-1 Multiplexer
0	0	A
0	1	B
1	0	C
1	1	D

Boolean Expression:

$$Vout = \overline{S_0 S_1} D_0 + S_0 \overline{S_1} D_1 + \overline{S_0} S_1 D_2 + S_0 S_1 D_3$$

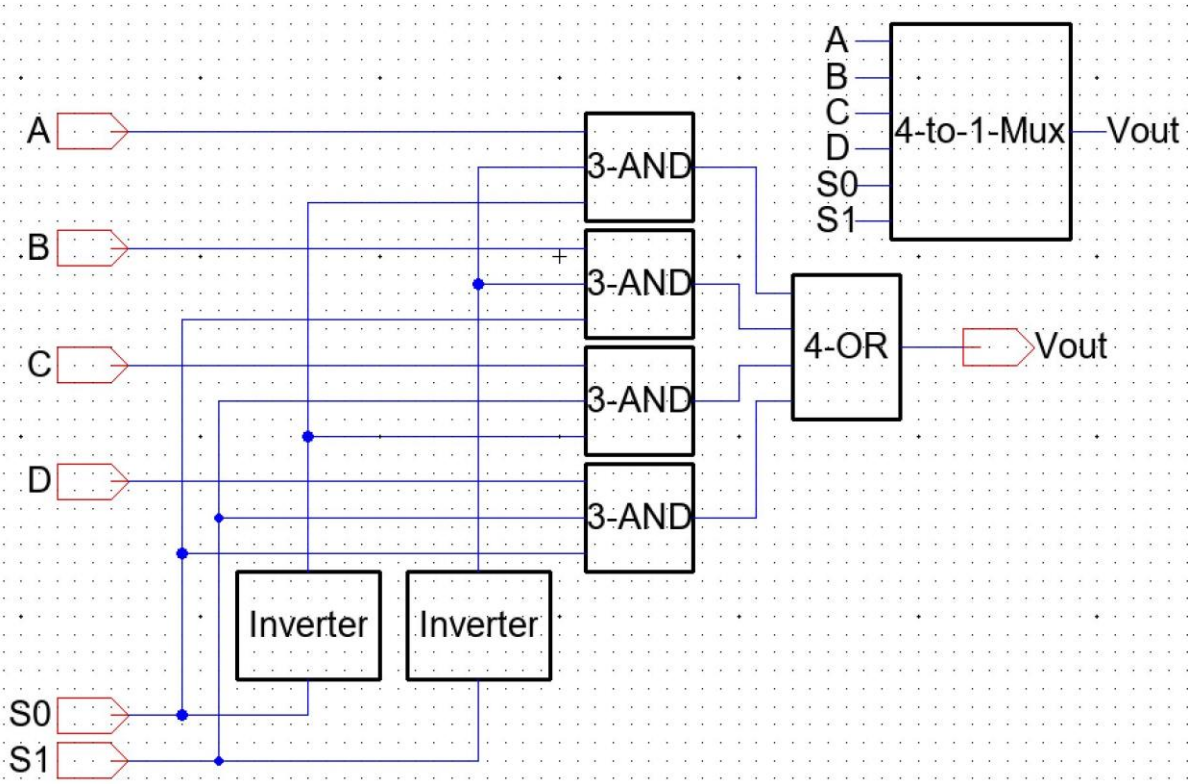

Figure 11: Schematic Design of a 4-to-1 Multiplexer

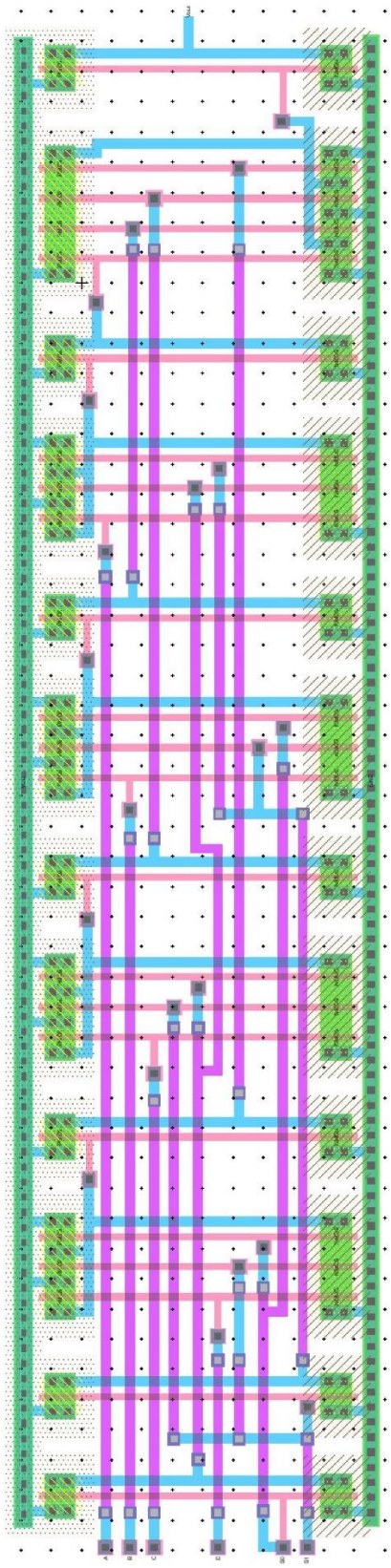

Figure 12.0: Layout Design of a 4-to-1 Multiplexer (Landscape)

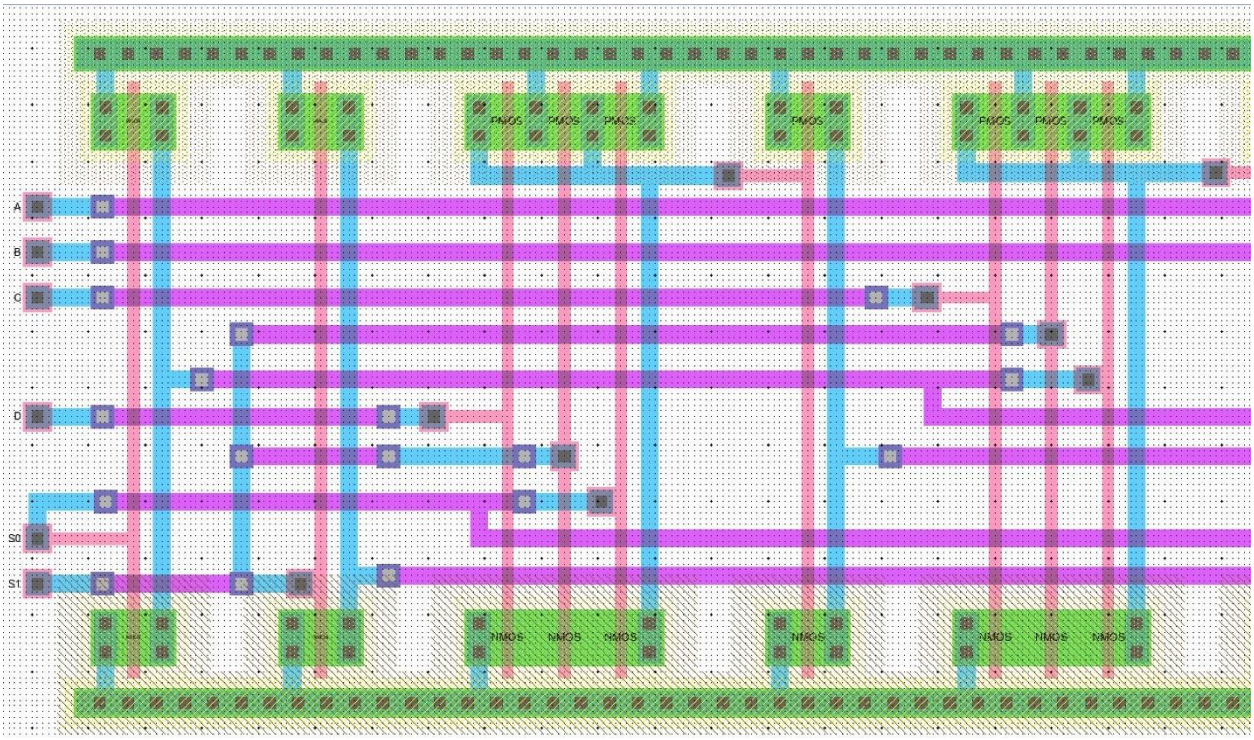

Figure 12.1: Layout Design of a 4-to-1 Multiplexer Zoomed (Left)

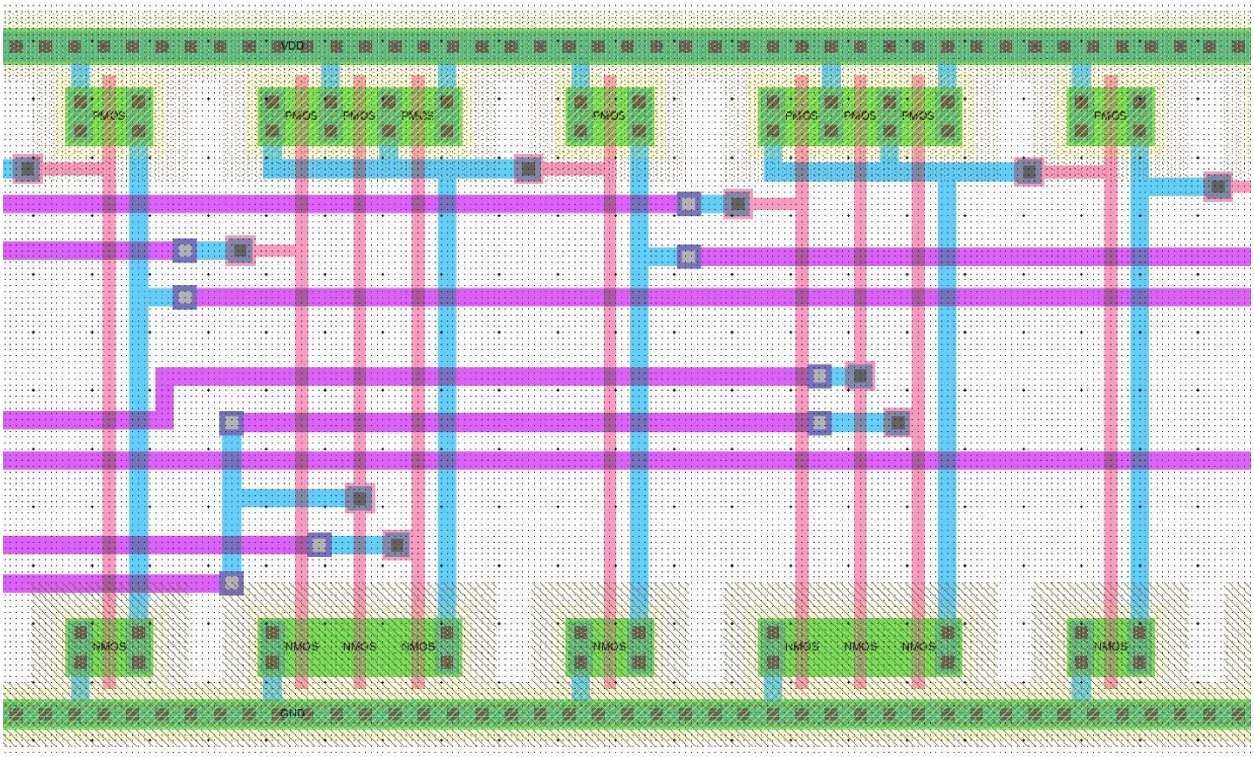

Figure 12.2: Layout Design of a 4-to-1 Multiplexer Zoomed (Middle)

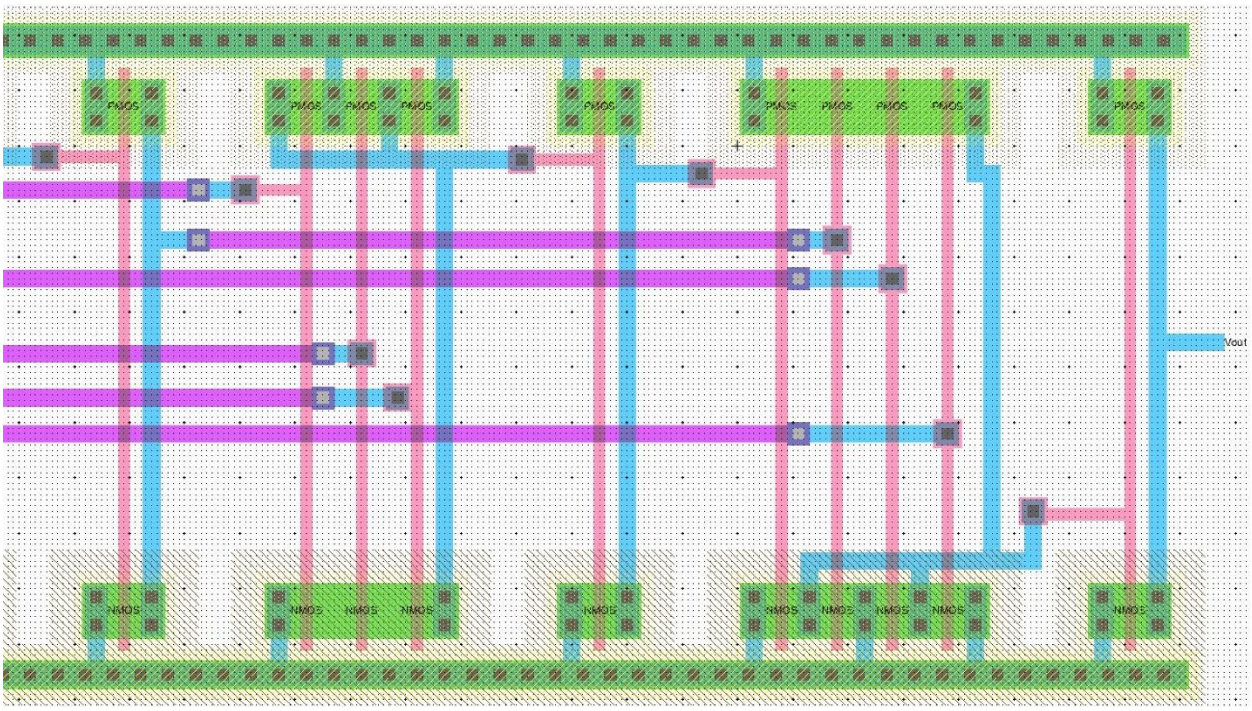

Figure 12.3: Layout Design of a 4-to-1 Multiplexer Zoomed (Right)

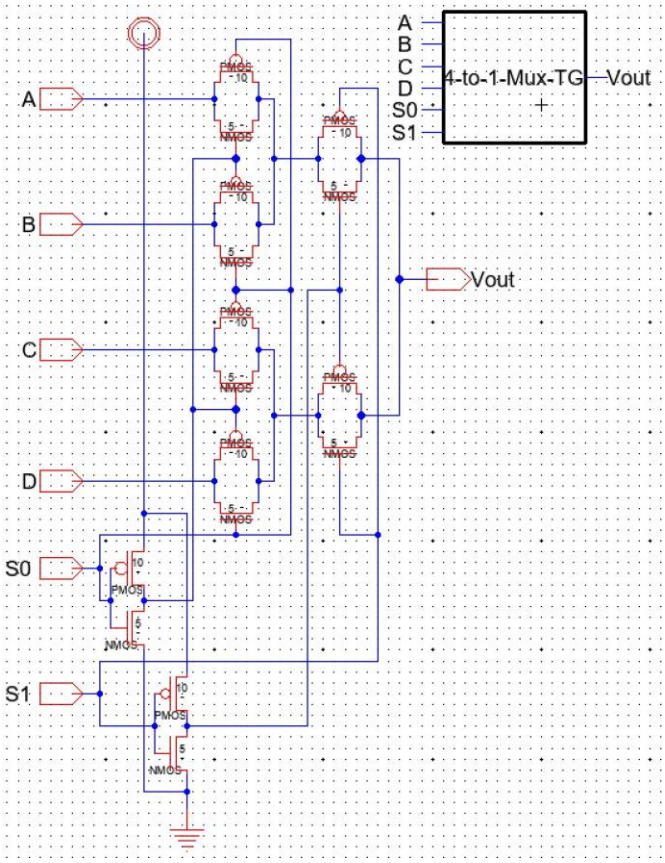

Figure 13: Schematic Design of a 4-to-1 Multiplexer Transmission Gate

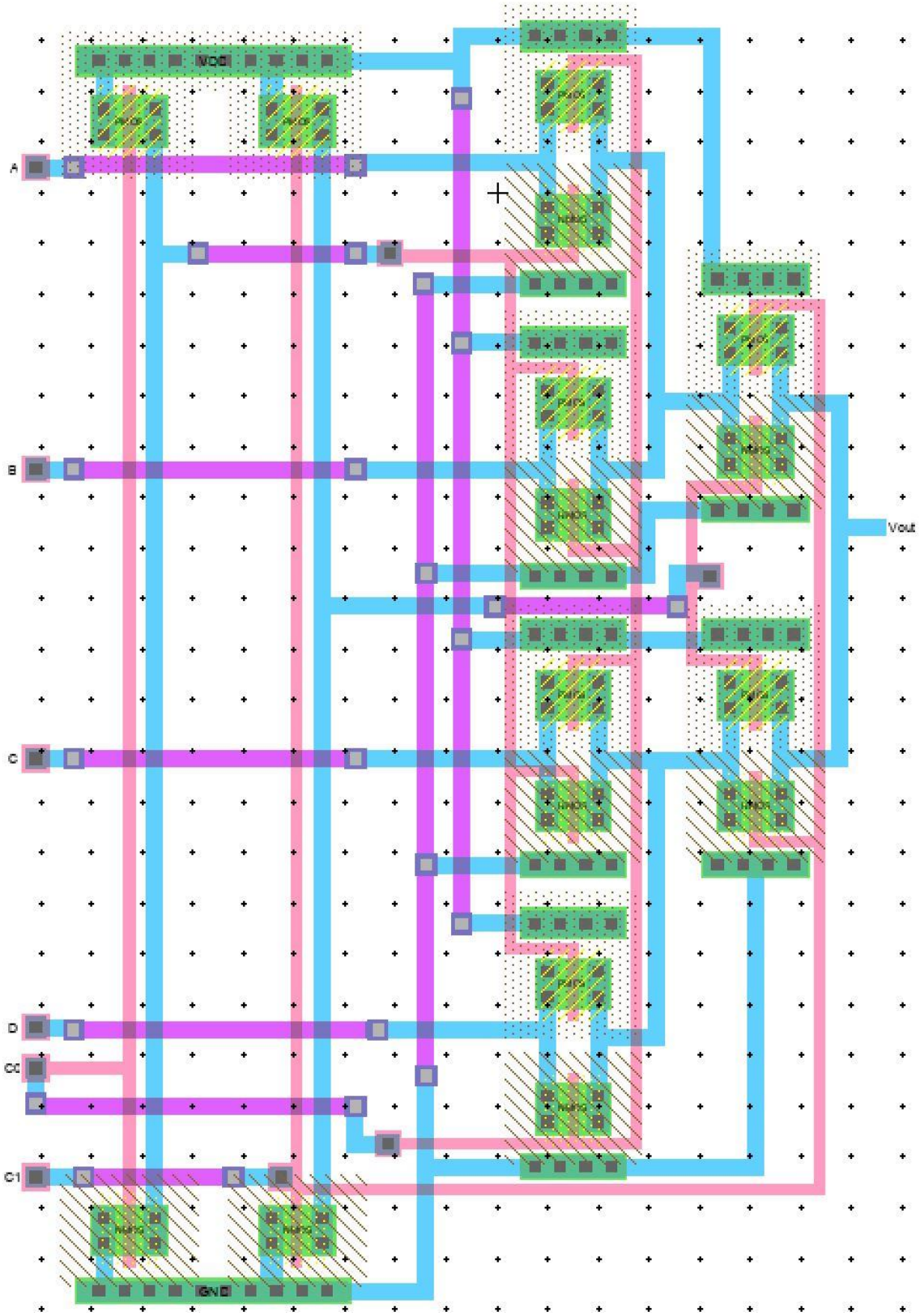

Figure 14.0: Layout Design of a 4-to-1 Multiplexer Transmission Gate

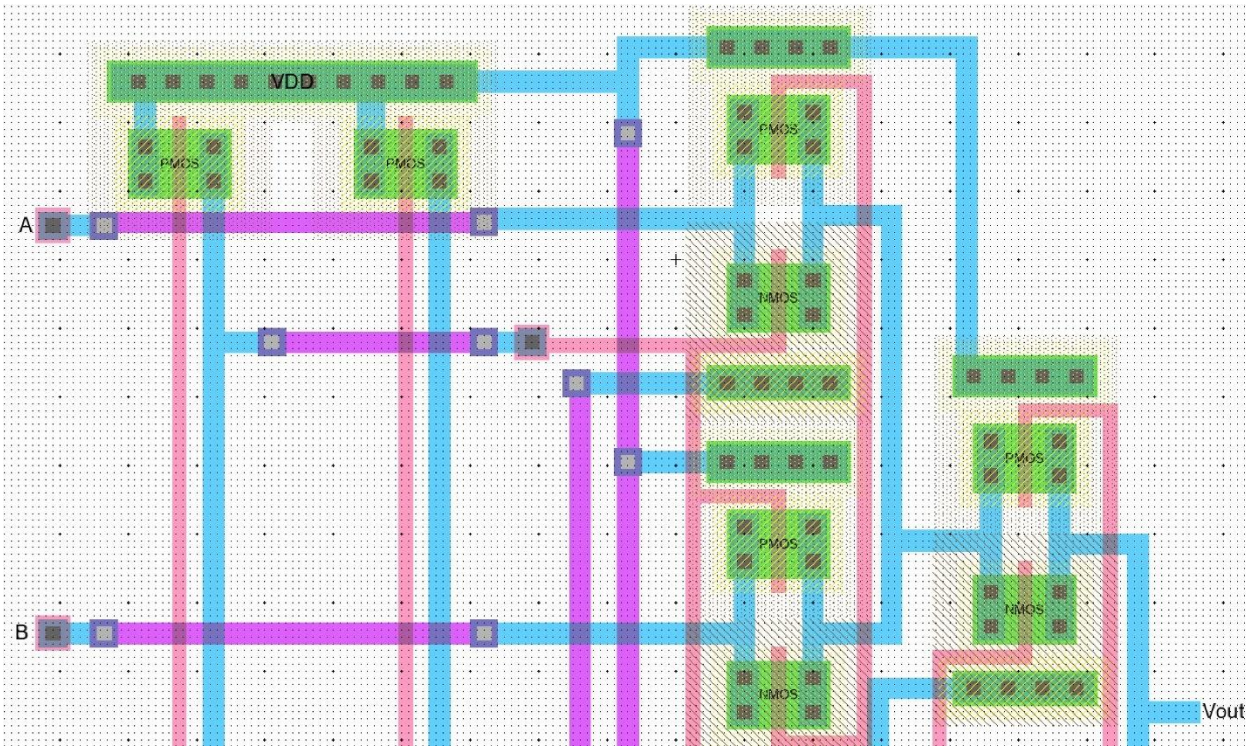

Figure 14.1: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Top)

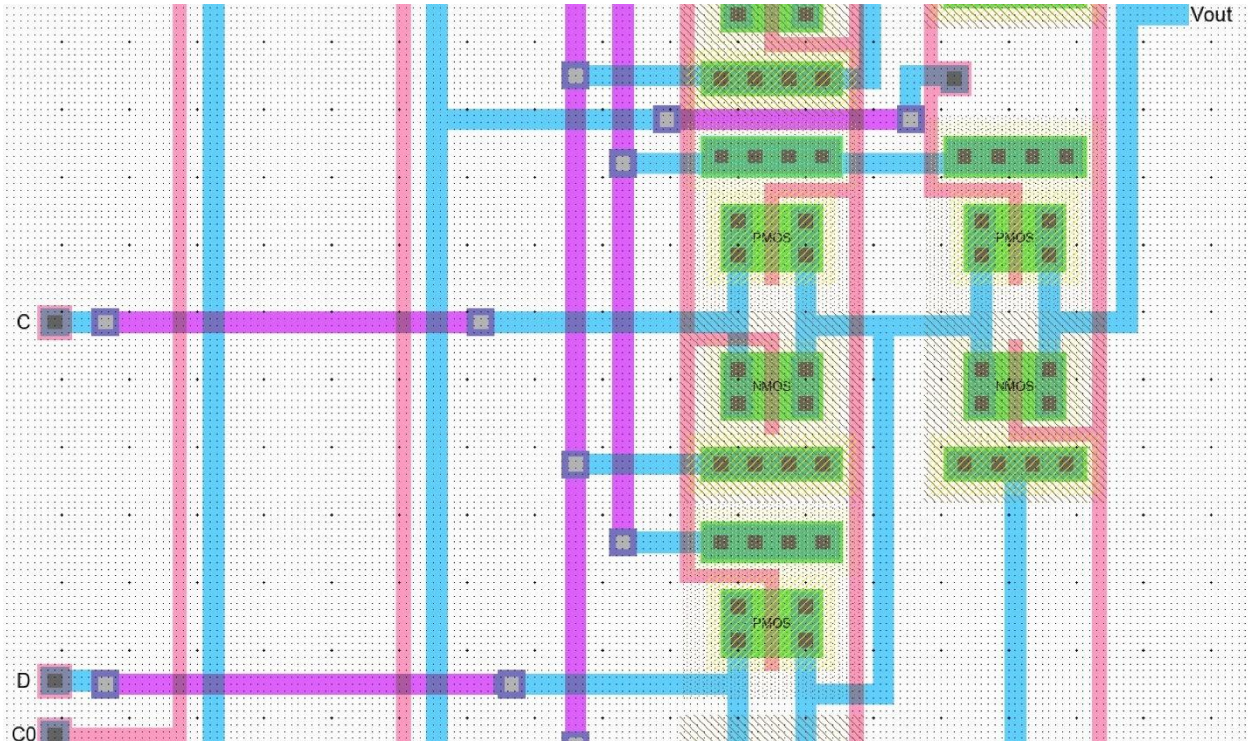

Figure 14.2: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Middle)

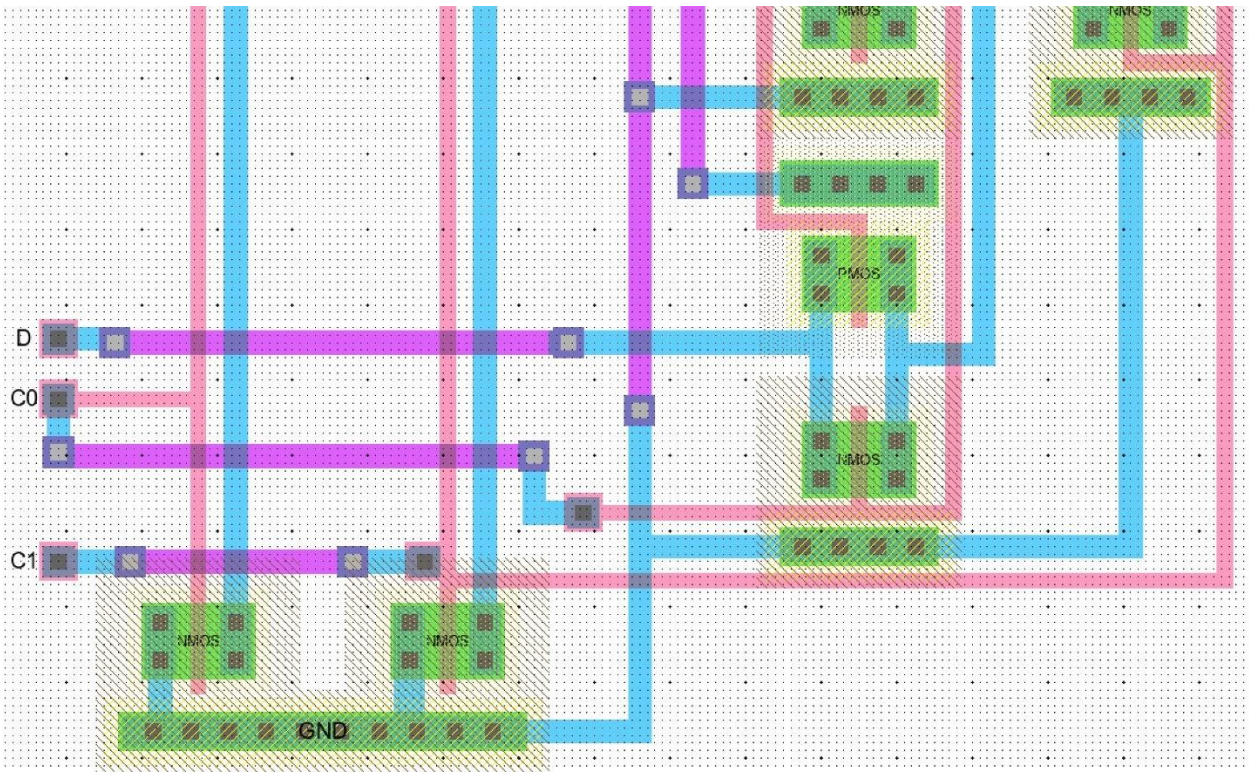

Figure 14.3: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Bottom)

Section 3: Electric Schematic:

We created a schematic of the conventional 16-to-1 Multiplexer by combining five 4-to-1 Multiplexers (Figure 11) together, using its icon. If there were any problems with the 4-to-1 Multiplexer, then we would have to go back to see the parts it was built from. In this case, the parts that it was built from are a two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, and an inverter. It was combined by connecting the output of four 4-to-1 Multiplexer to the four inputs on another 4-to-1 Multiplexer. Figure 15 shows the schematic design that was built using Electric of the conventional 16-to-1 Multiplexer. Figure 16 shows the Design Rule Check (DRC) that was performed on the schematic for the conventional 16-to-1 Multiplexer; it indicates that there were no errors or warning with the schematic.

For the transmission gate 16-to-1 Multiplexer, it's created by combining five transmission gate 4-to-1 Multiplexer (Figure 13). It was combined by connecting the output of four transmission gate 4-to-1 Multiplexer to the four inputs on another transmission gate 4-to-1 Multiplexer. Figure 17 shows the schematic design that was built using Electric of the transmission gate 16-to-1 Multiplexer. Figure 18 shows the Design Rule Check (DRC) that was performed on the schematic for the transmission gate 16-to-1 Multiplexer; it indicates that there were no errors or warning with the schematic.

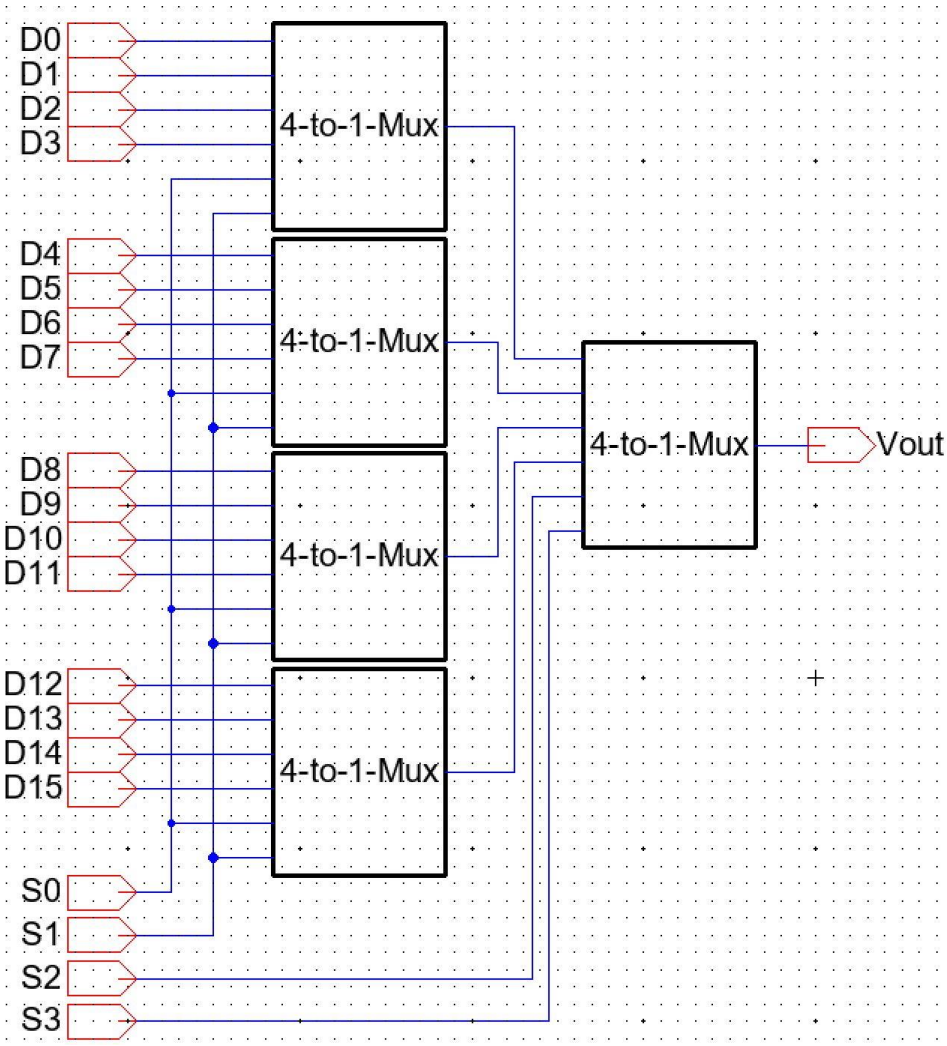

Figure 15: Schematic Design of a 16-to-1 Multiplexer

Electric Messages

```
================================5================================
Checking schematic cell 'AND{sch}'
   No errors found
Checking schematic cell '3-AND{sch}'
   No errors found
Checking schematic cell 'OR{sch}'
   No errors found
Checking schematic cell '4-OR{sch}'
   No errors found
Checking schematic cell 'Inverter{sch}'
   No errors found
Checking schematic cell '4-to-1-Mux{sch}'
   No errors found
Checking schematic cell '16-to-1-Mux{sch}'
   No errors found
0 errors and 0 warnings found (took 0.031 secs)
```

Figure 16: Design Rule Check (DRC) of a 16-to-1 Multiplexer Schematic Design

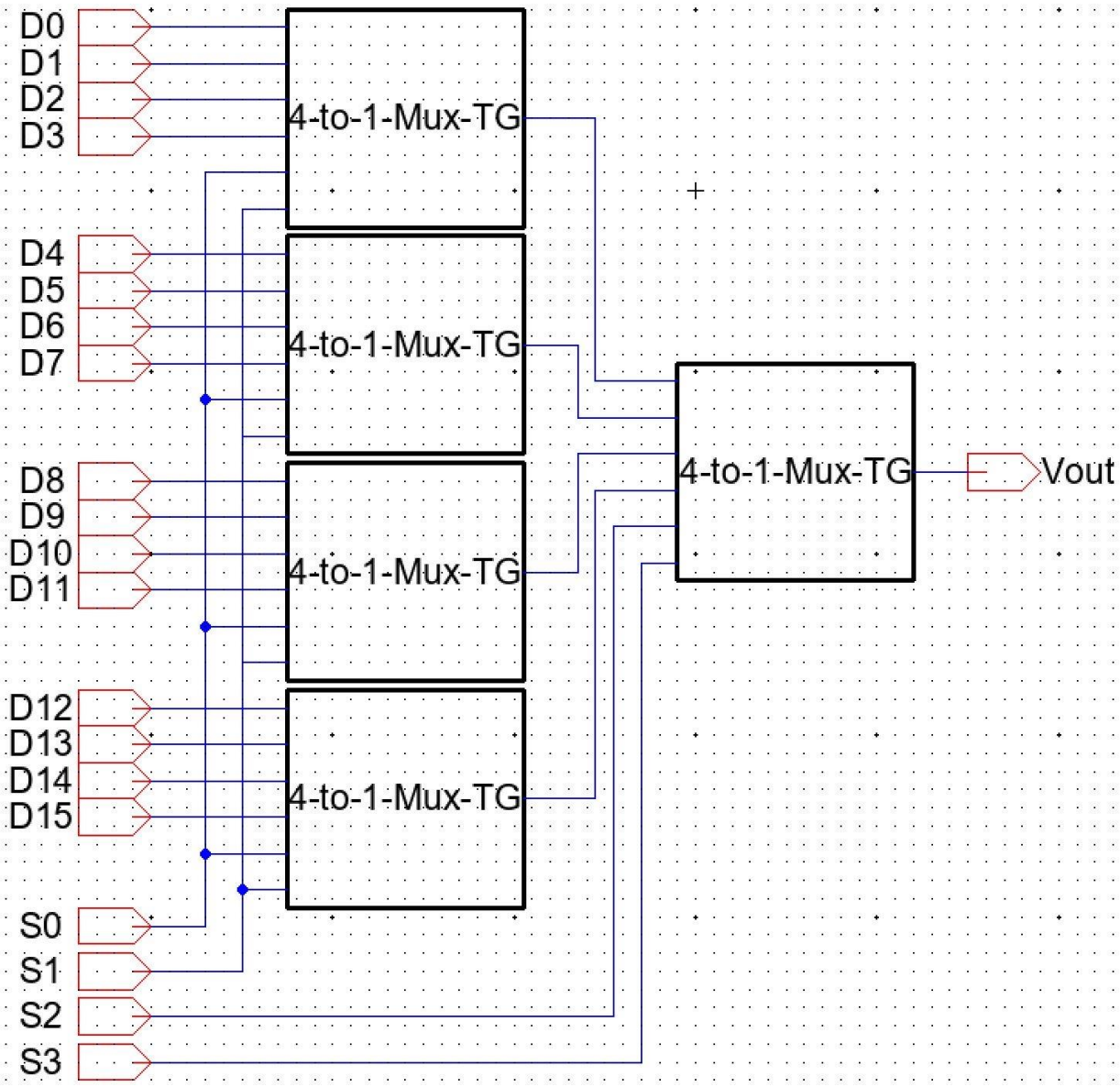

Figure 17: Schematic Design of a 16-to-1 Multiplexer Transmission Gate

Electric Messages

```
================================9================================
Checking schematic cell '4-to-1-Mux-TG{sch}'
   No errors found
Checking schematic cell '16-to-1-Mux-TG{sch}'
   No errors found
0 errors and 0 warnings found (took 0.031 secs)
```

Figure 18: Design Rule Check (DRC) of a 16-to-1 Multiplexer Transmission Gate Schematic Design

Section 4: Electric Layout:

We created a layout of the conventional 16-to-1 Multiplexer by combining five 4-to-1 Multiplexers (Figure 12) together. If there were any problems with the 4-to-1 Multiplexer, then we would have to go back to see the parts it was built from. In this case, the parts that it was built from are a two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, and an inverter. It was combined by connecting the output of four 4-to-1 Multiplexer to the four inputs on another 4-to-1 Multiplexer. Figure 19 shows the layout design that was built using Electric of the conventional 16-to-1 Multiplexer. There is an overview and a zoomed version of the layout since the overview isn't clear enough. In addition, if additional justifications are needed, refer to Figure 12. Figure 20 shows the Design Rule Check (DRC) and Well Check that was performed on the layout for the conventional 16-to-1 Multiplexer; it indicates that there were no errors or warning with the layout.

For the transmission gate 16-to-1 Multiplexer, it's created by combining five transmission gate 4-to-1 Multiplexer (Figure 14). It was combined by connecting the output of four transmission gate 4-to-1 Multiplexer to the four inputs on another transmission gate 4-to-1 Multiplexer. Figure 21 shows the layout design that was built using Electric of the transmission gate 16-to-1 Multiplexer. There is an overview and a zoomed version of the layout since the overview isn't clear enough. In addition, if additional justifications are needed, refer to Figure 14. Figure 22 shows the Design Rule Check (DRC) and Well Check that was performed on the layout for the transmission gate 16-to-1 Multiplexer; it indicates that there were no errors or warning with the layout.

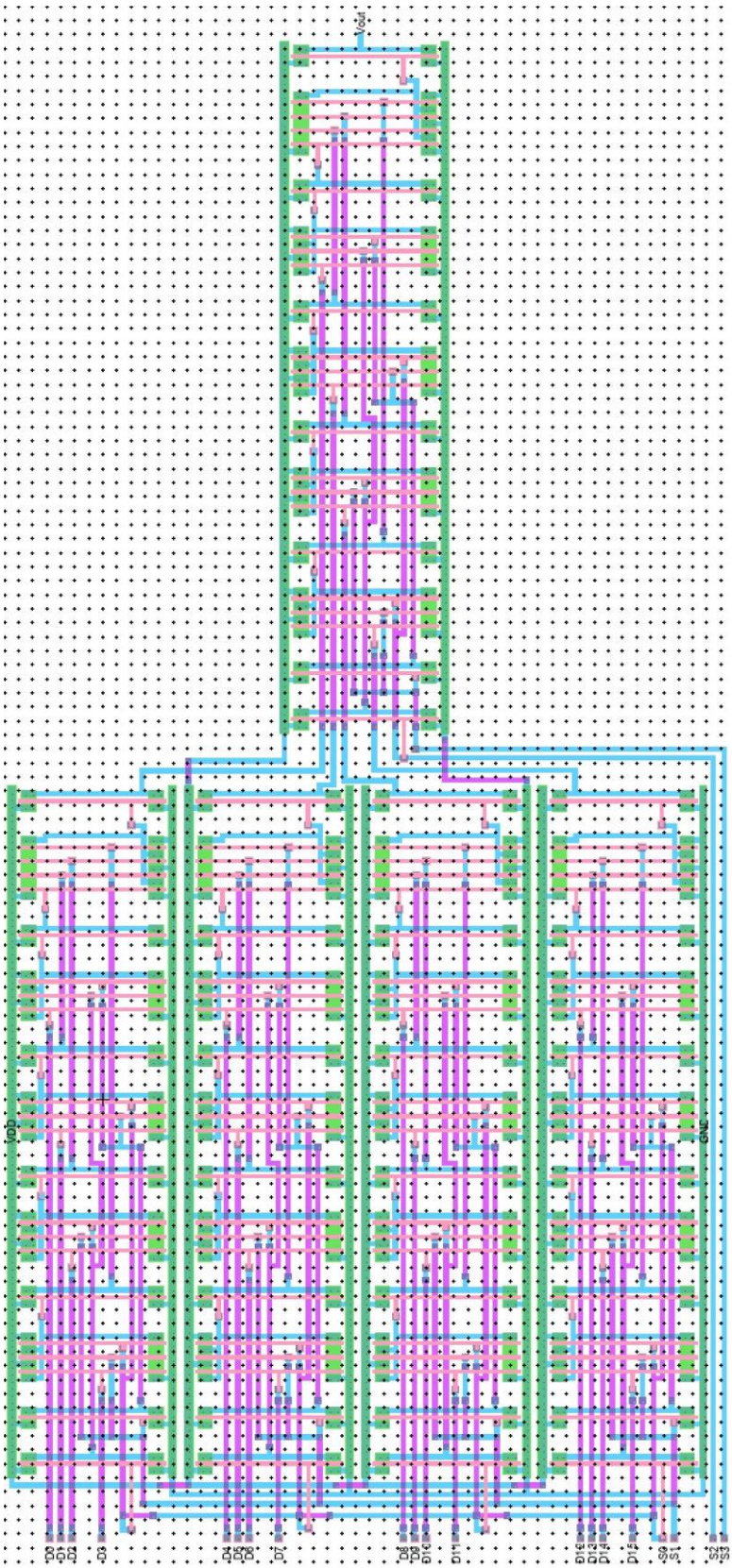

Figure 19.0: Layout Design of a 16-to-1 Multiplexer (Landscape)

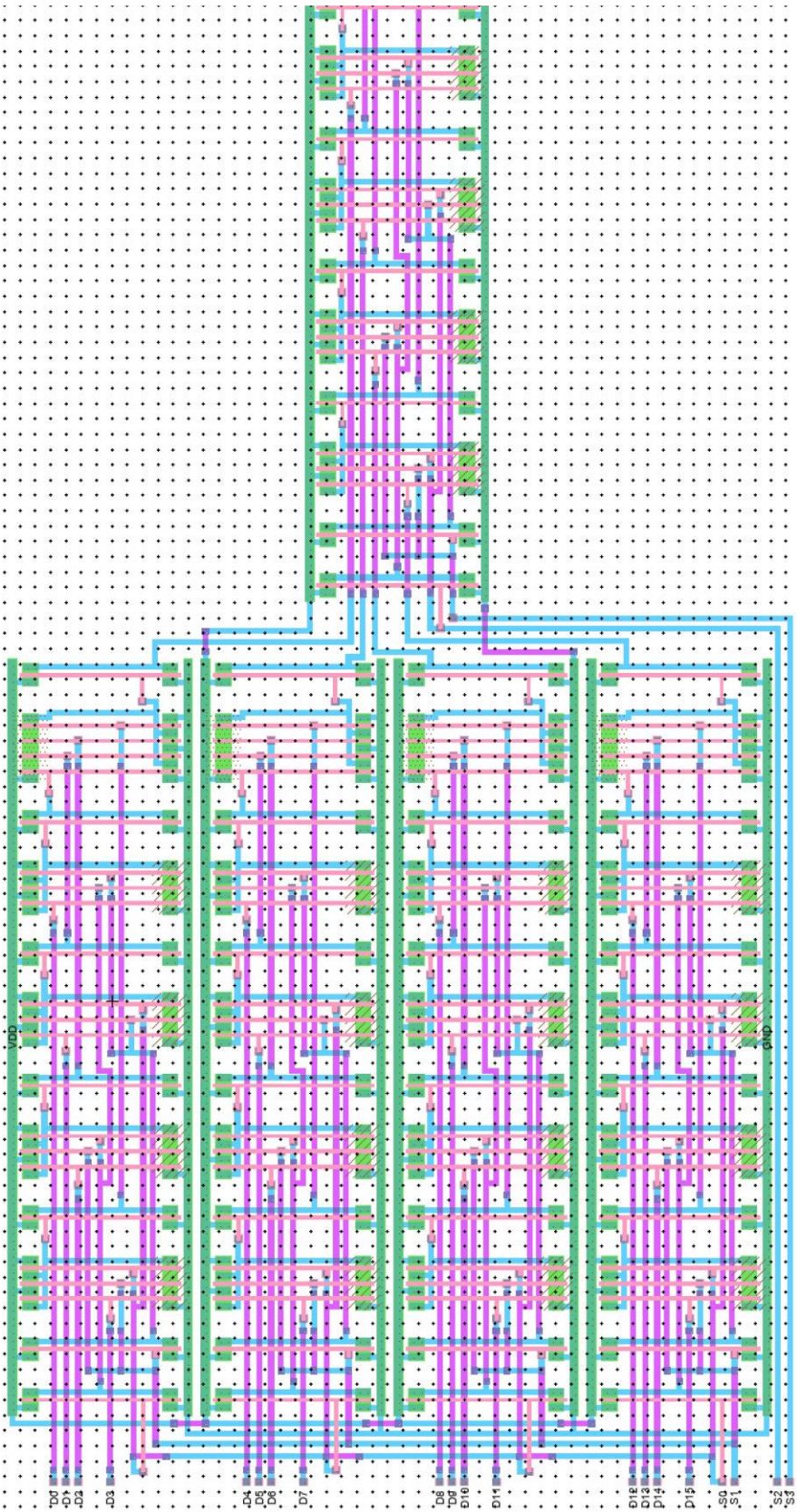

Figure 19.1: Layout Design of a 16-to-1 Multiplexer Zoomed (Landscape)

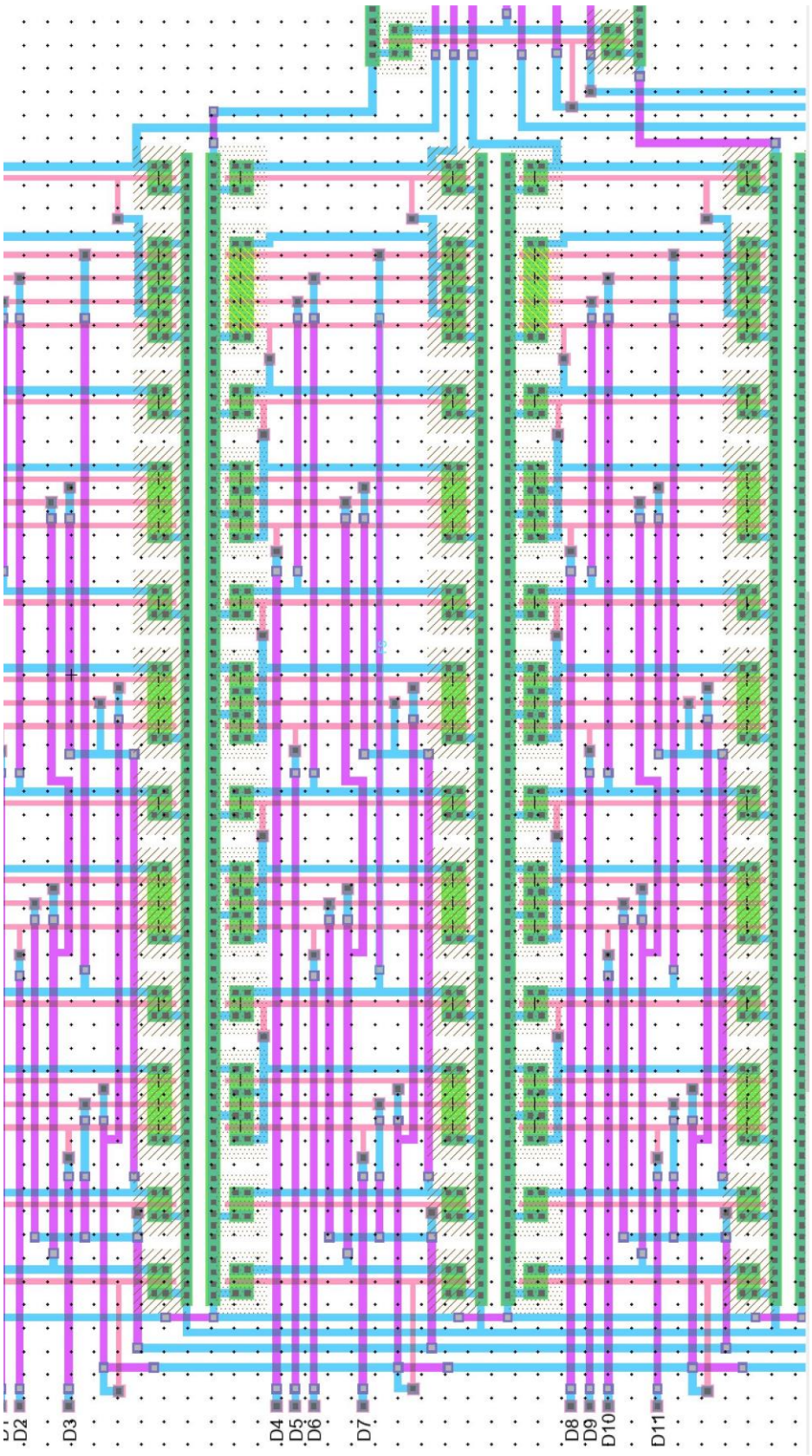

Figure 19.2: Layout Design of a 16-to-1 Multiplexer Zoomed (Landscape)

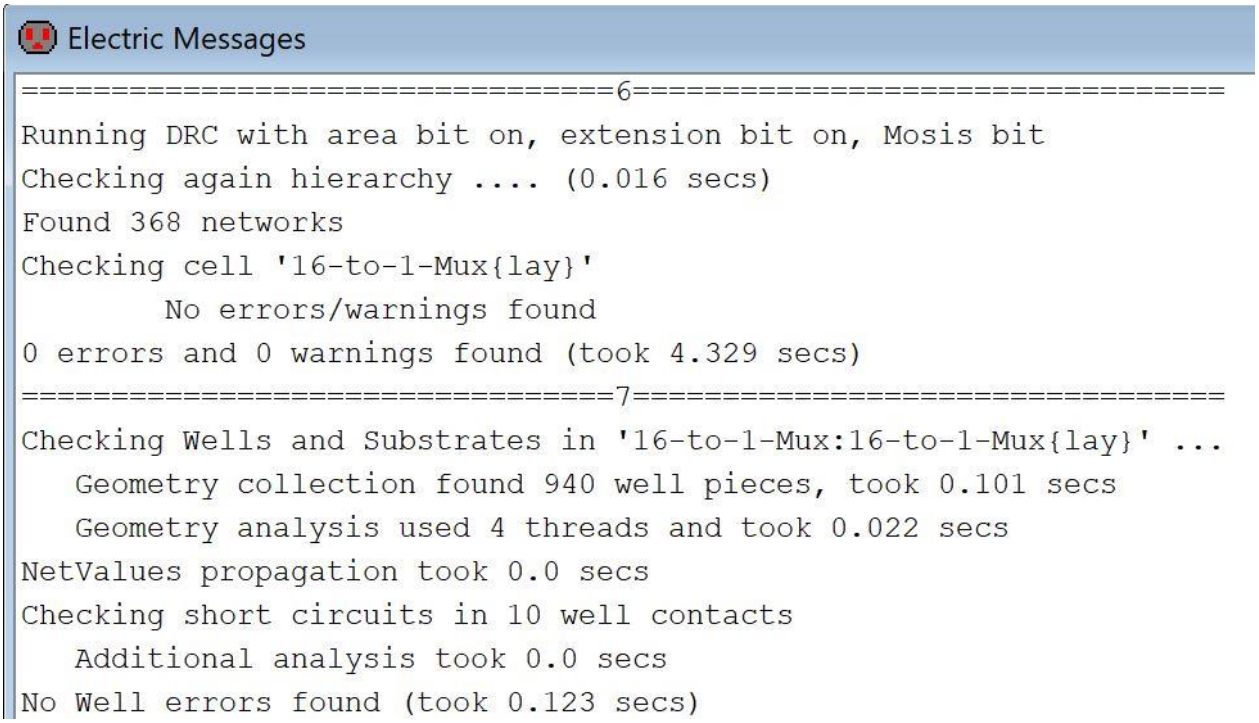

Figure 20: Design Rule Check (DRC) and Well Check of a 16-to-1 Multiplexer Layout Design

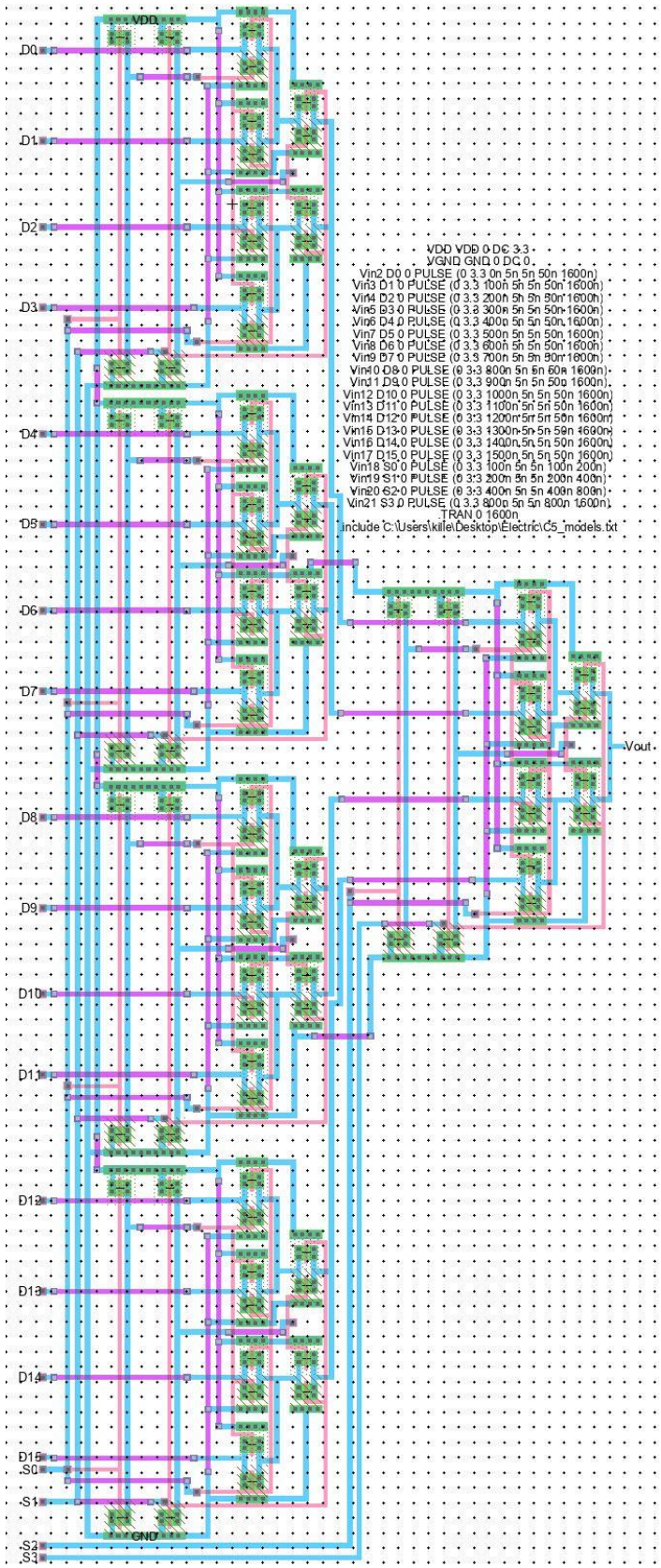

Figure 21.0: Layout Design of a Transmission Gate 16-to-1 Multiplexer

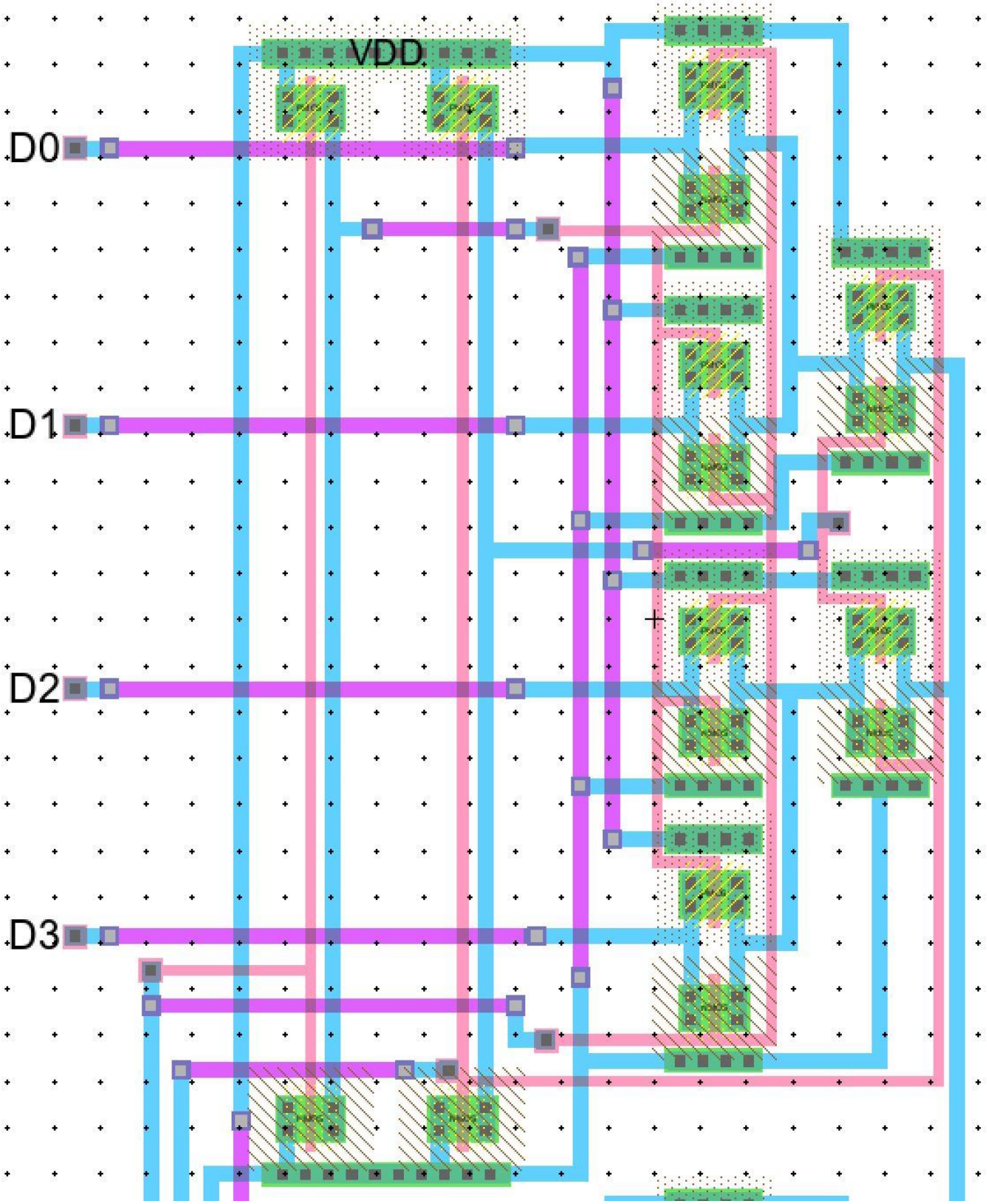

Figure 21.1: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Top)

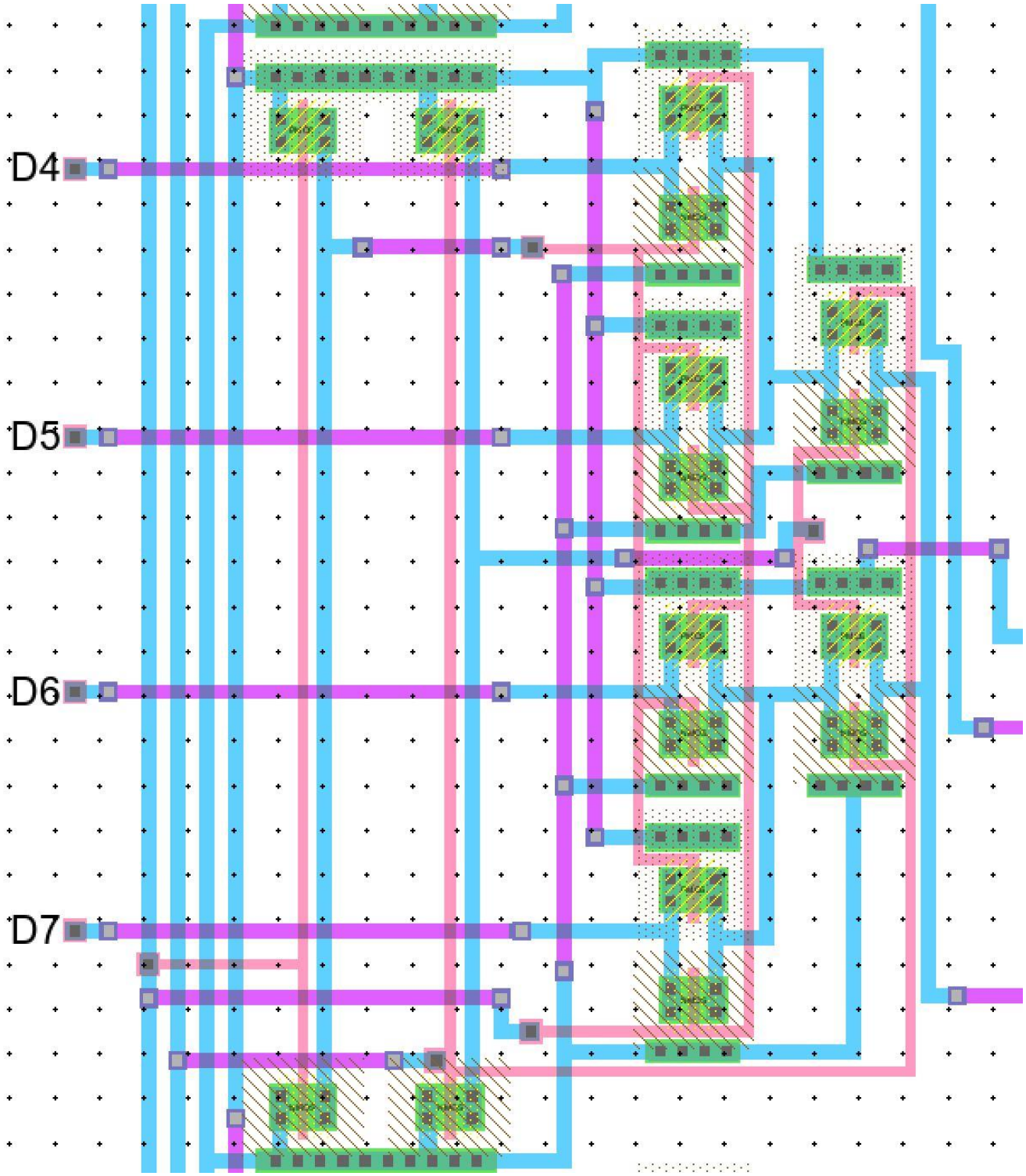

Figure 21.2: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle Left)

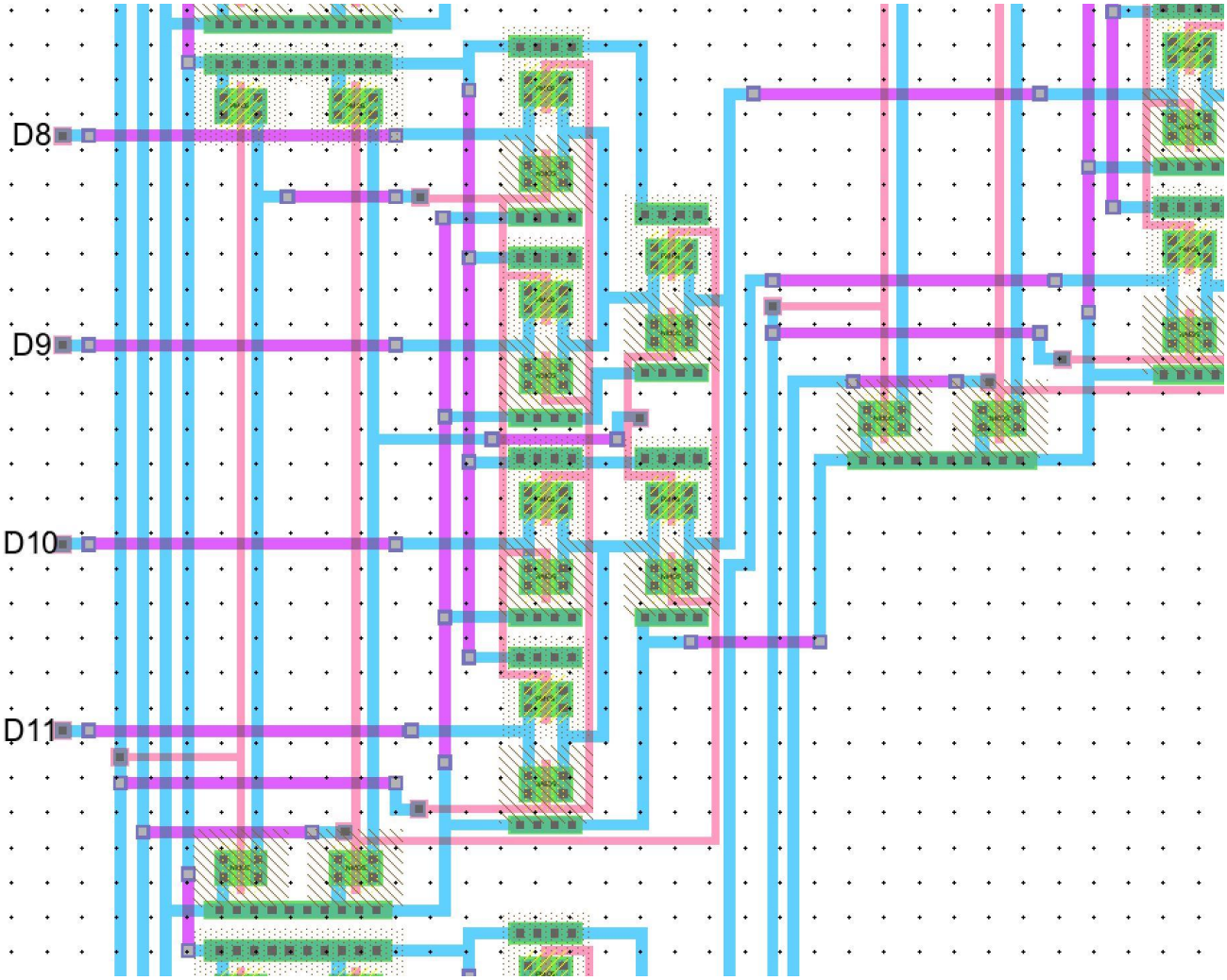

Figure 21.3: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle Left)

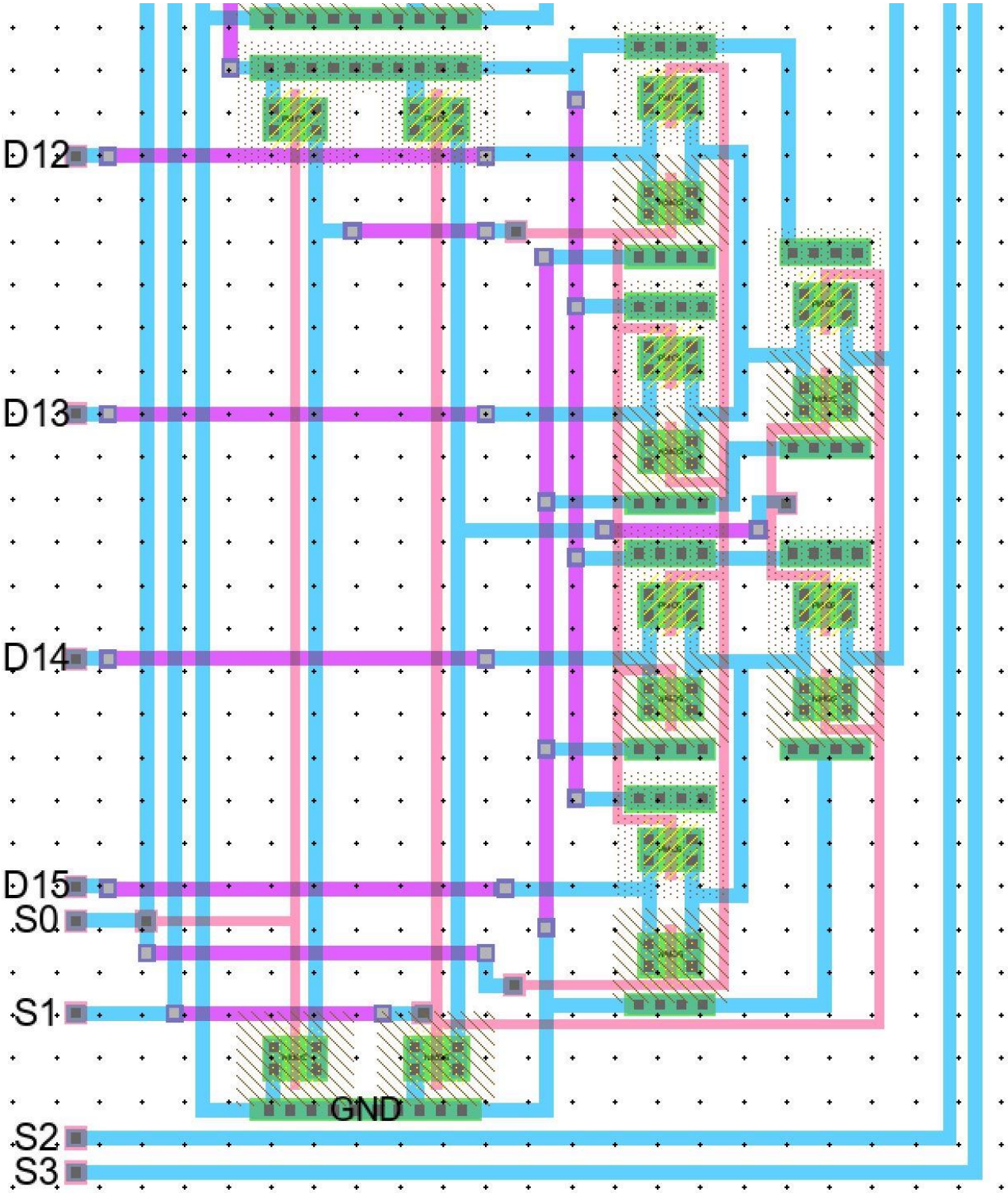

Figure 21.4: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Bottom)

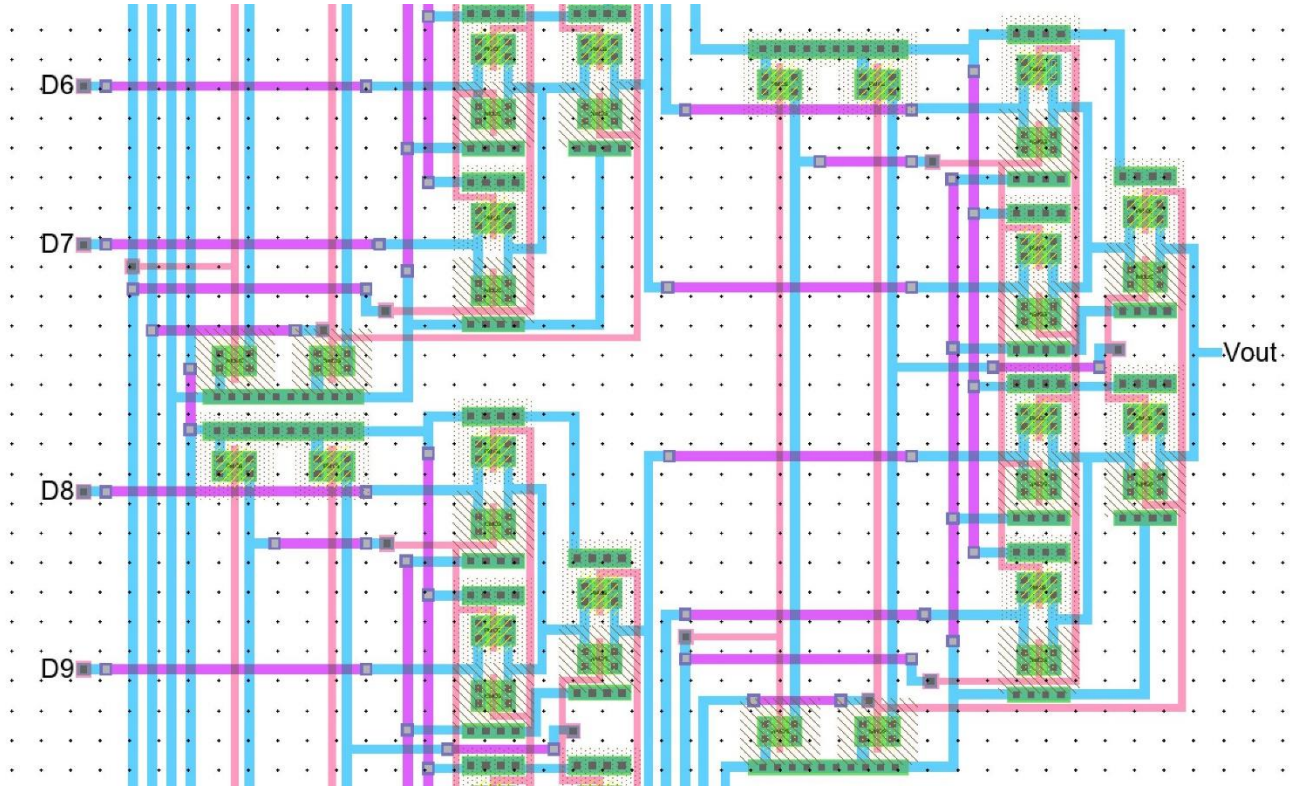

Figure 21.5: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle)

Electric Messages

```
================================10================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 128 networks
Checking cell '16-to-1-Mux-TG{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 1.108 secs)
================================11================================
Checking Wells and Substrates in '16-to-1-Mux:16-to-1-Mux-TG{lay}' ...
   Geometry collection found 470 well pieces, took 0.015 secs
   Geometry analysis used 4 threads and took 0.022 secs
NetValues propagation took 0.0 secs
Checking short circuits in 70 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.037 secs)
```

Figure 22: Design Rule Check (DRC) and Well Check of a Transmission Gate 16-to-1 Multiplexer Layout Design

Section 5: IRSIM Simulations:

After creating the schematic and layout design of the 16-to-1 Multiplexer, waveforms were created using IRSIM. Theses waveforms were created by configuring the inputs, D0-D15, and S0-S3, so that it could test certain computations. The computations that it tested are the same between the schematic and layout. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify the waveforms obtained from IRSIM were correct by matching it with the truth table on Table 1.

Section 5.1: Schematic:

For the schematic, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the selectors and counting the peaks for the one that's selected and comparing it with the output.

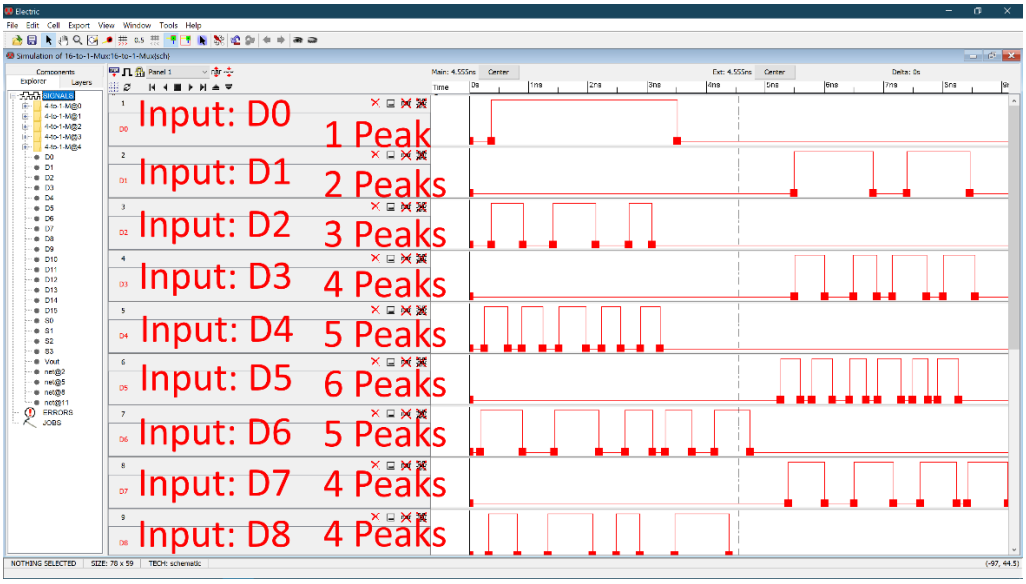

Figure 23.1: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer

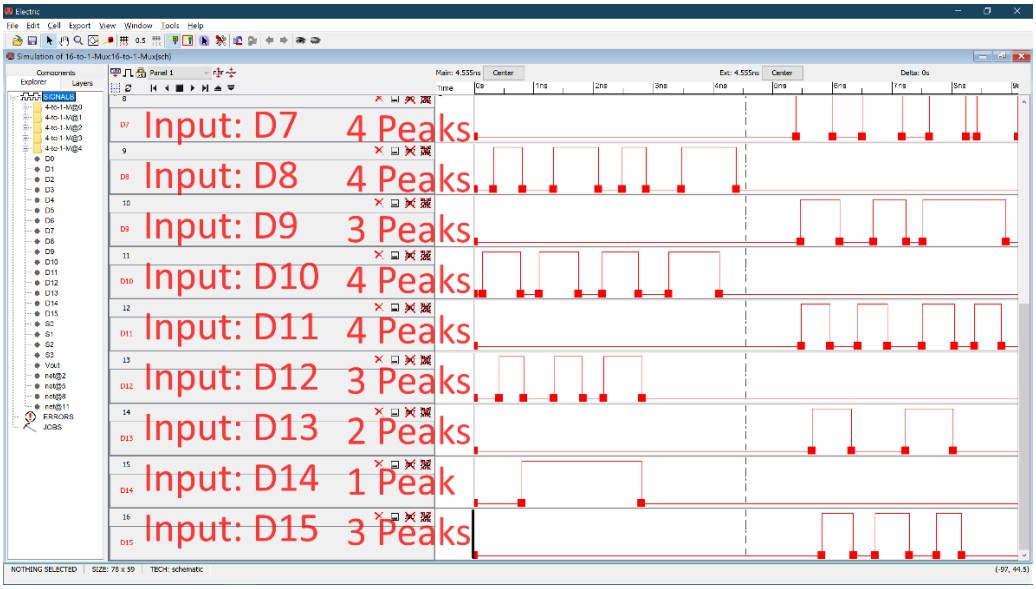

Figure 23.2: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer

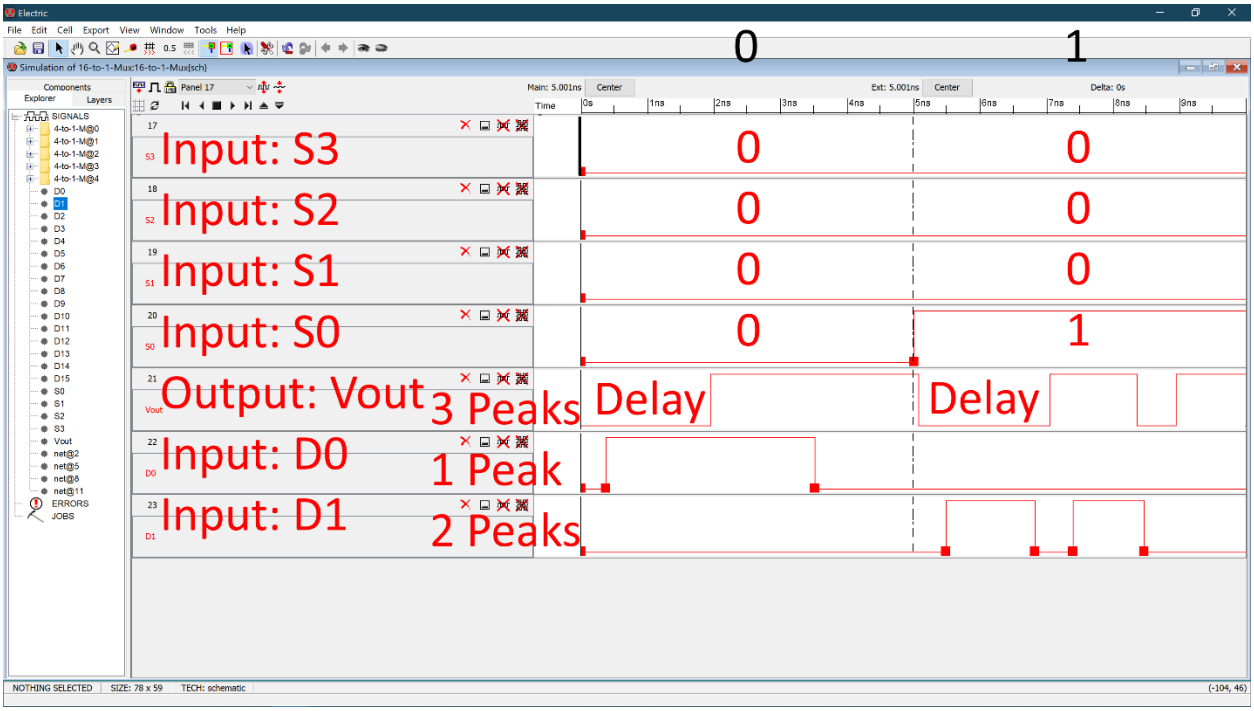

Figure 23.3: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 0 and 1)

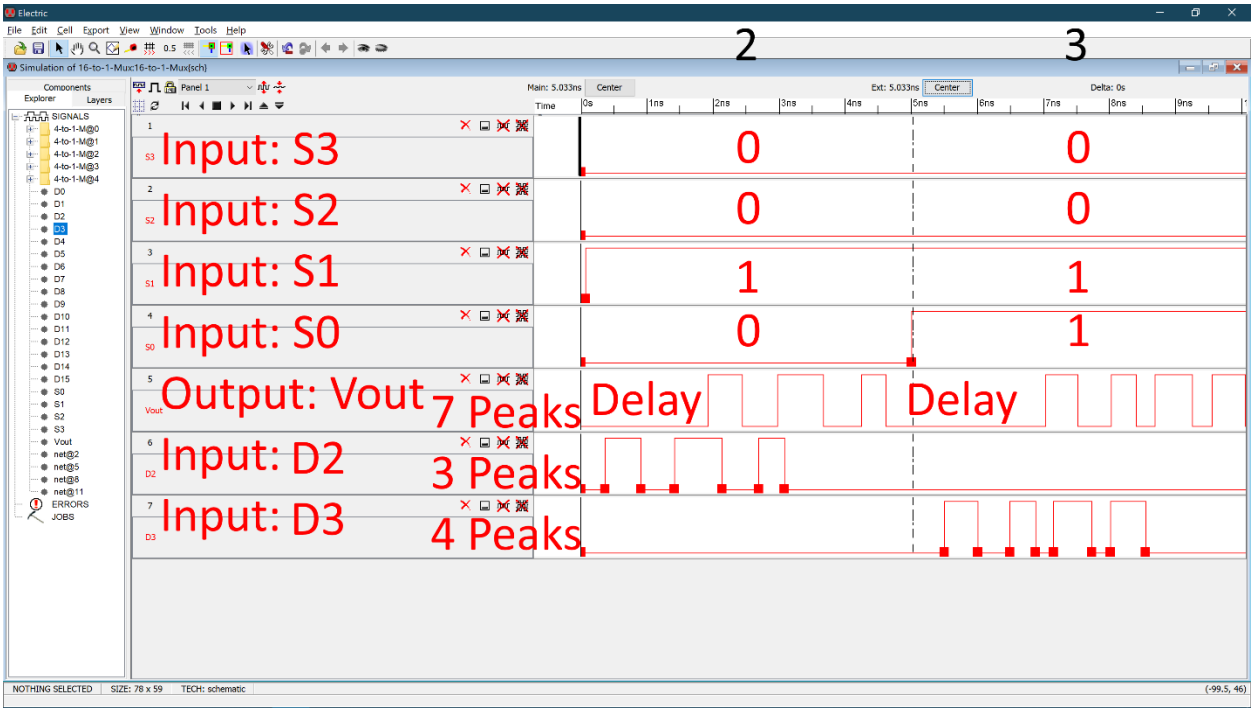

Figure 23.4: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 2 and 3)

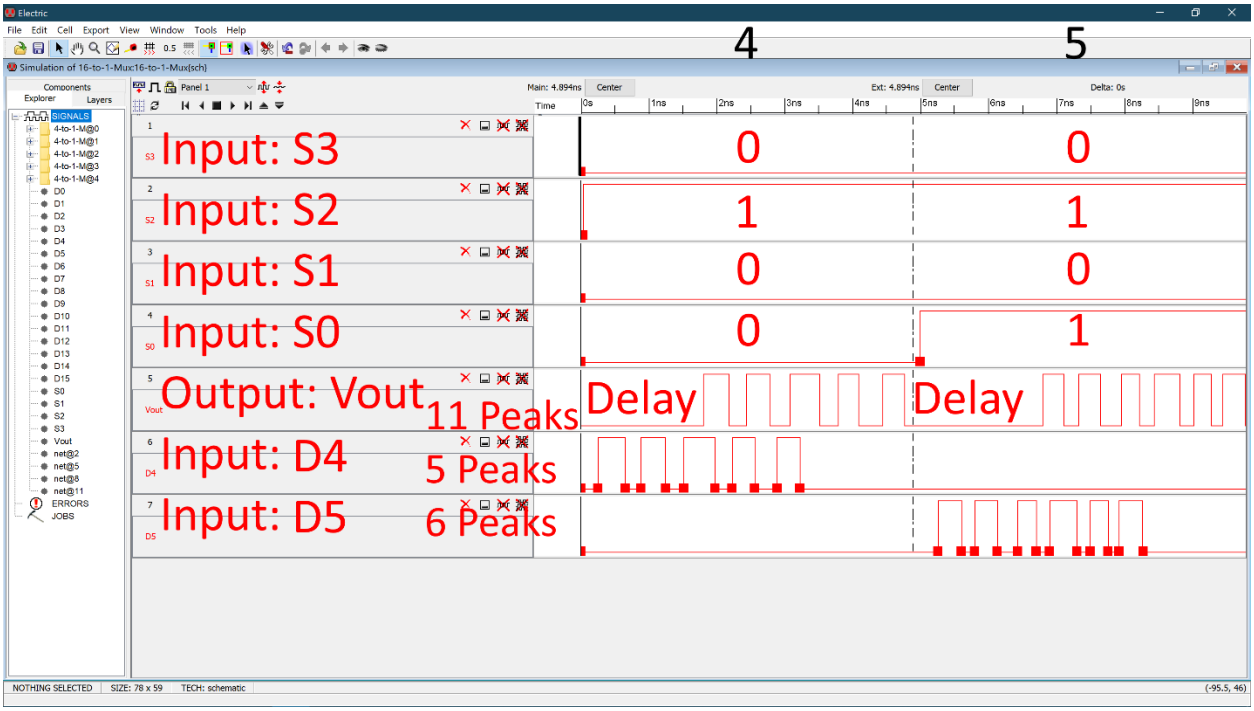

Figure 23.5: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 4 and 5)

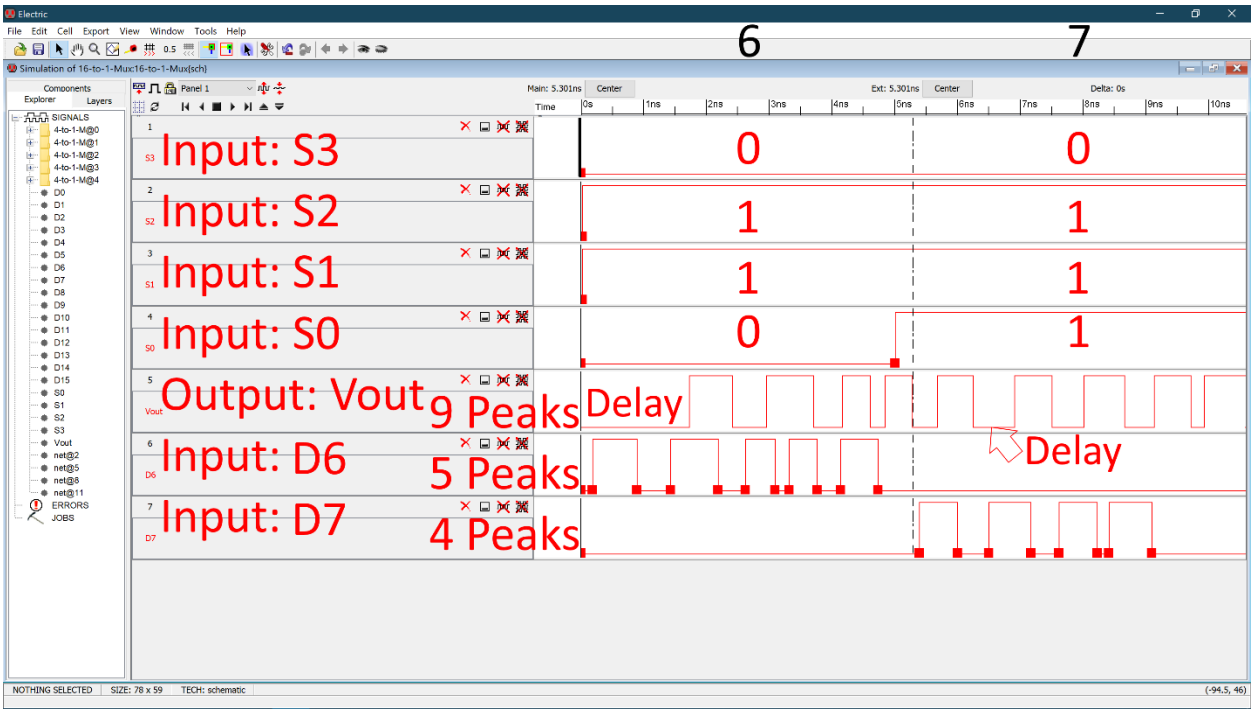

Figure 23.6: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 6 and 7)

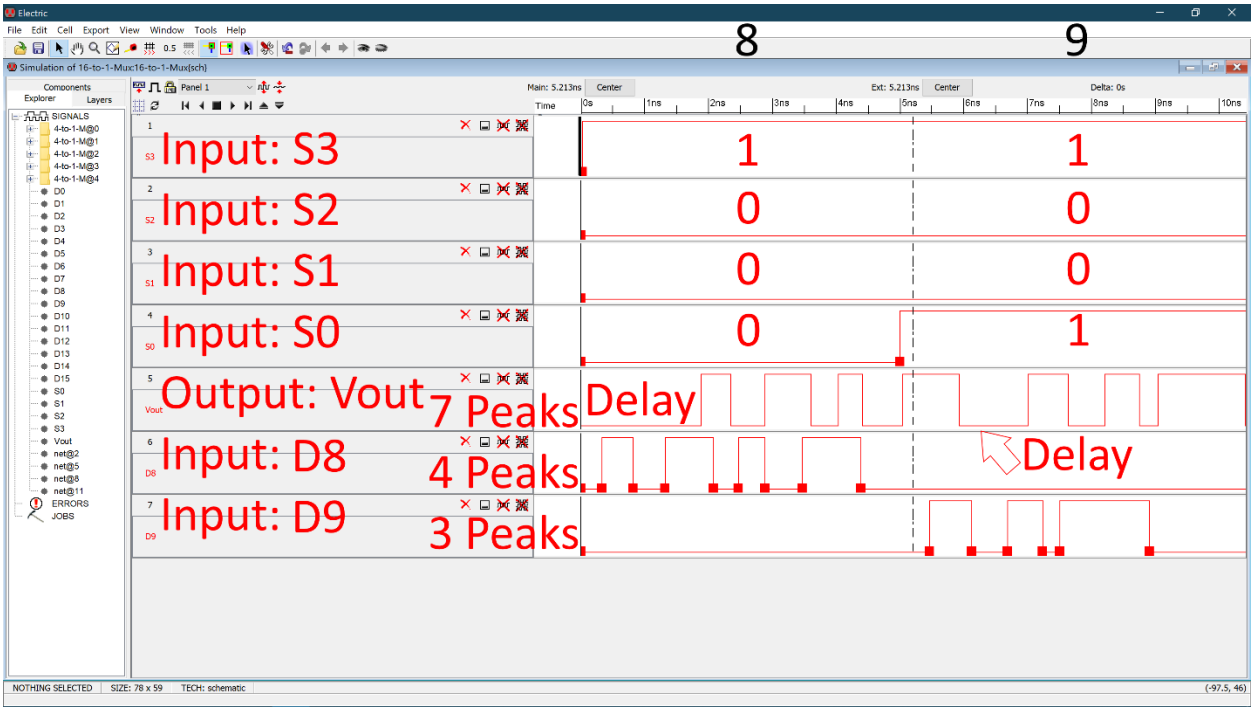

Figure 23.7: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 8 and 9)

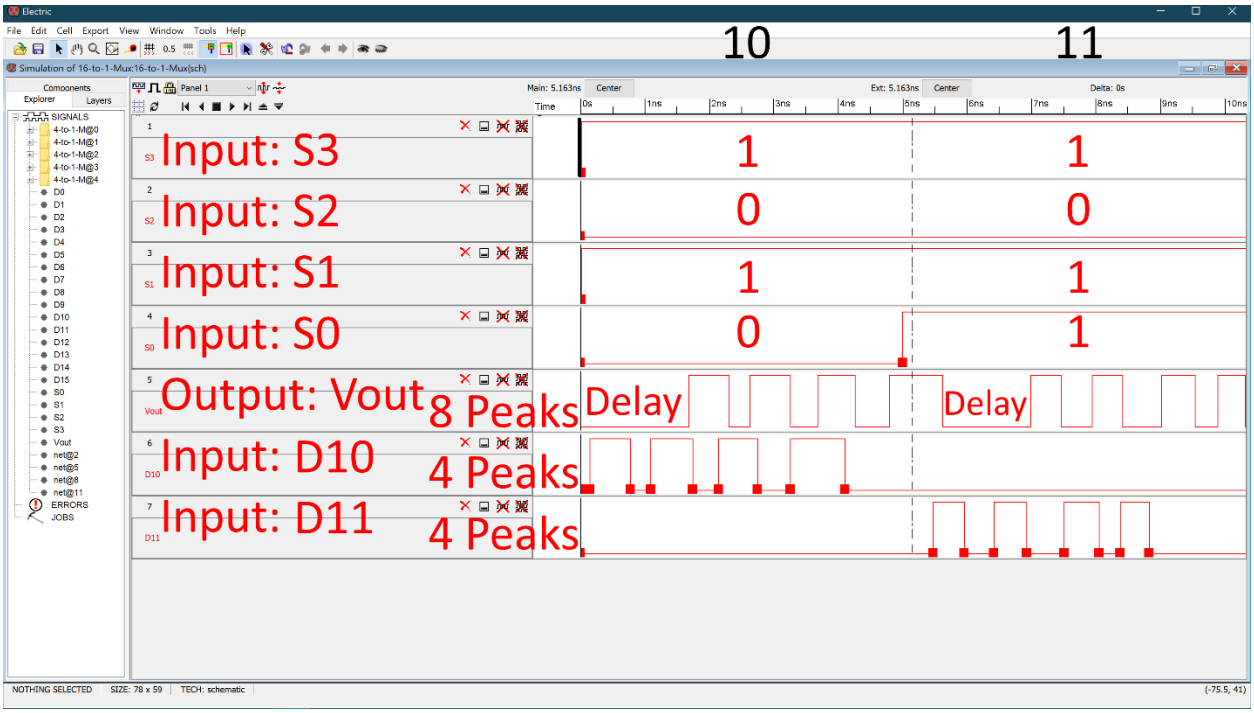

Figure 23.8: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 10 and 11)

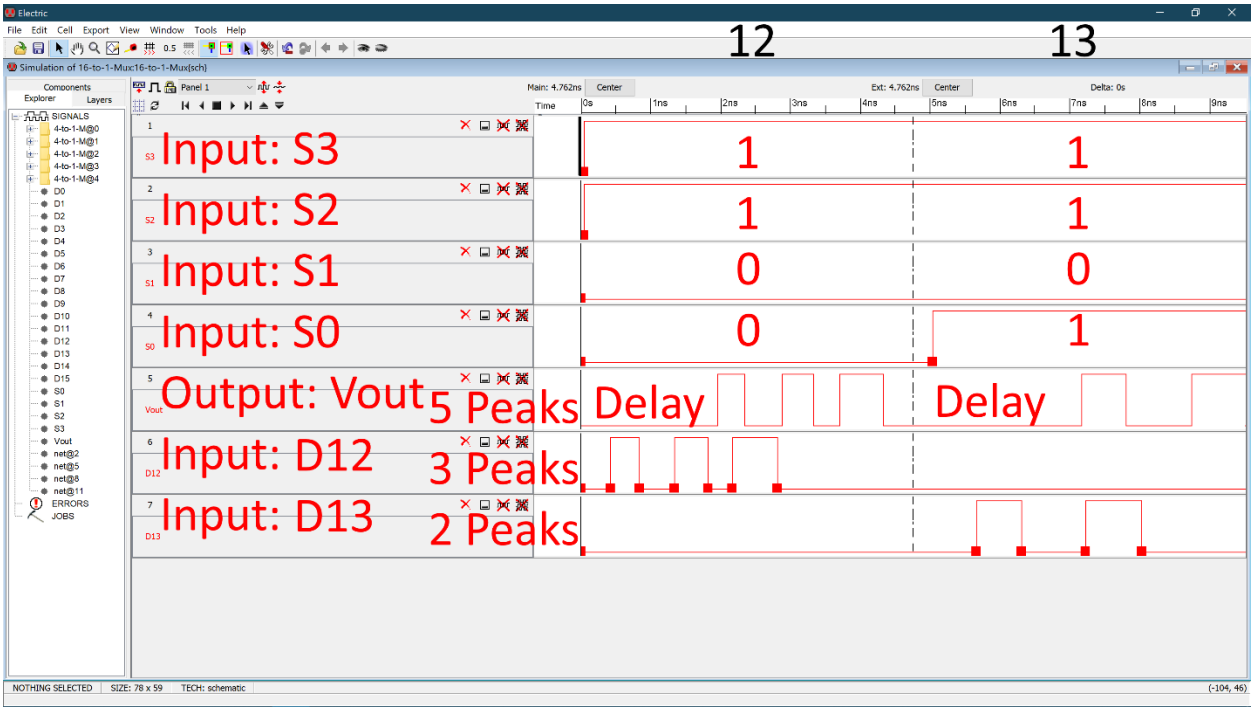

Figure 23.9: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 12 and 13)

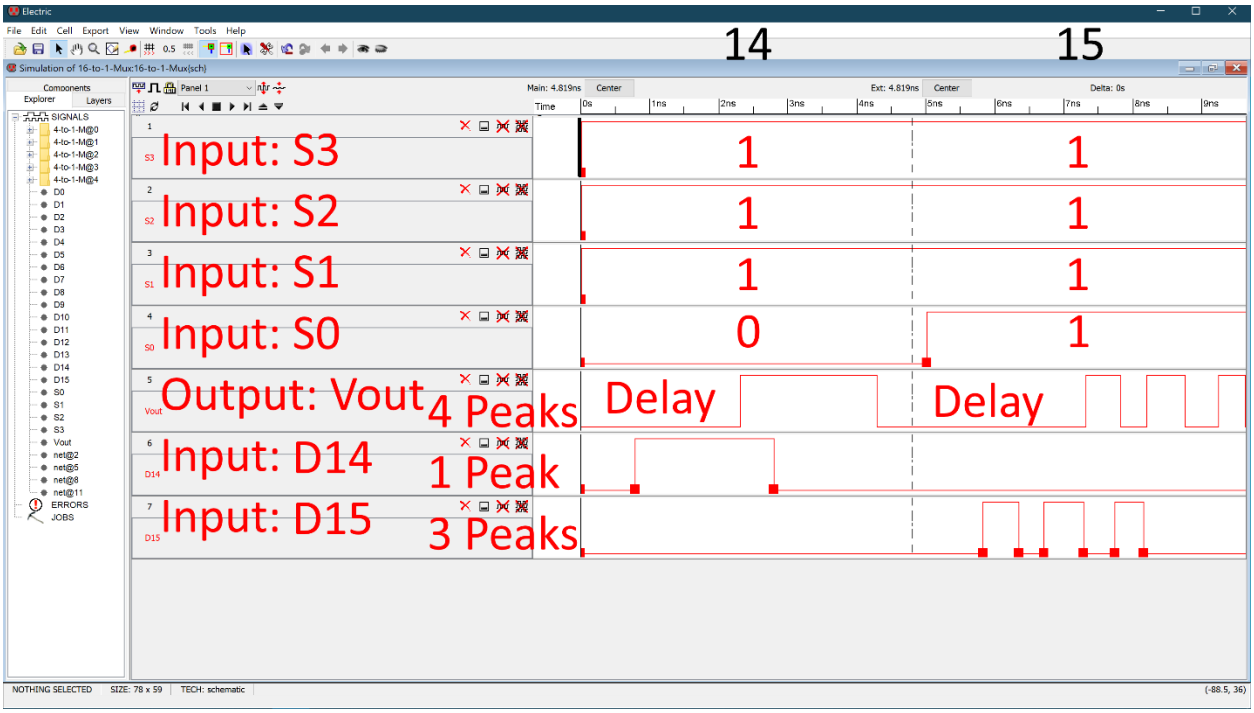

Figure 23.10: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 14 and 15)

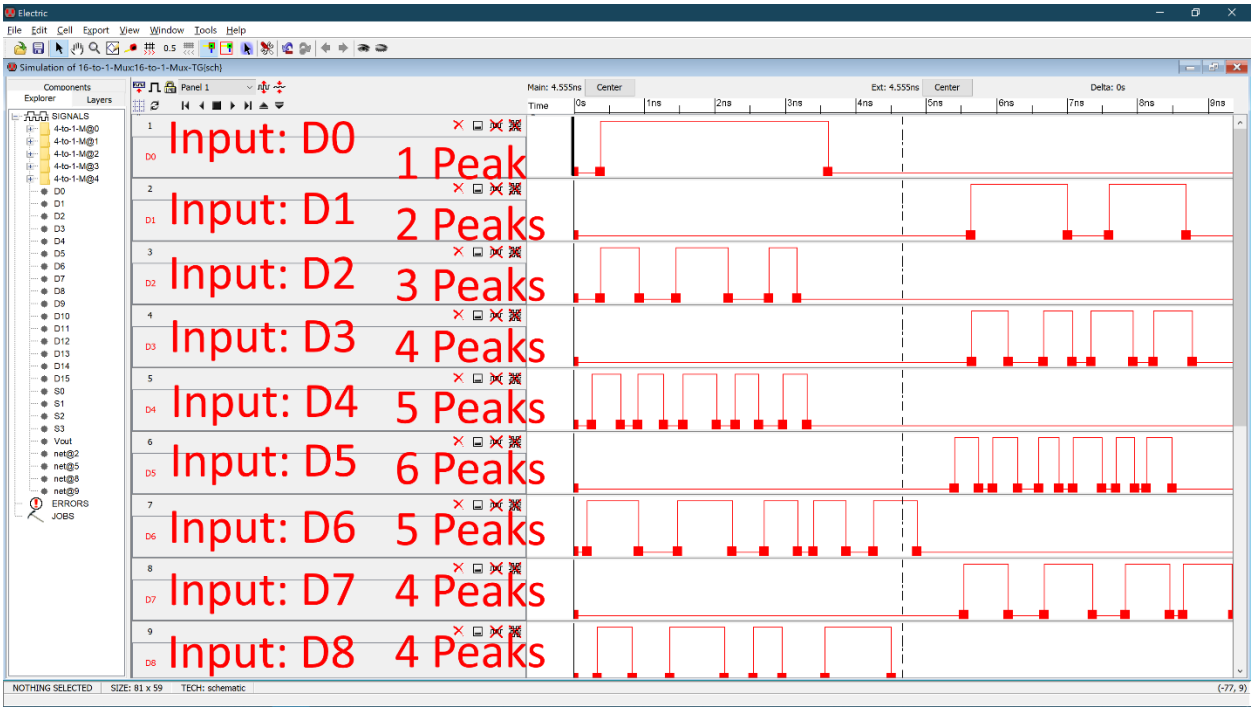

Figure 24.1: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer

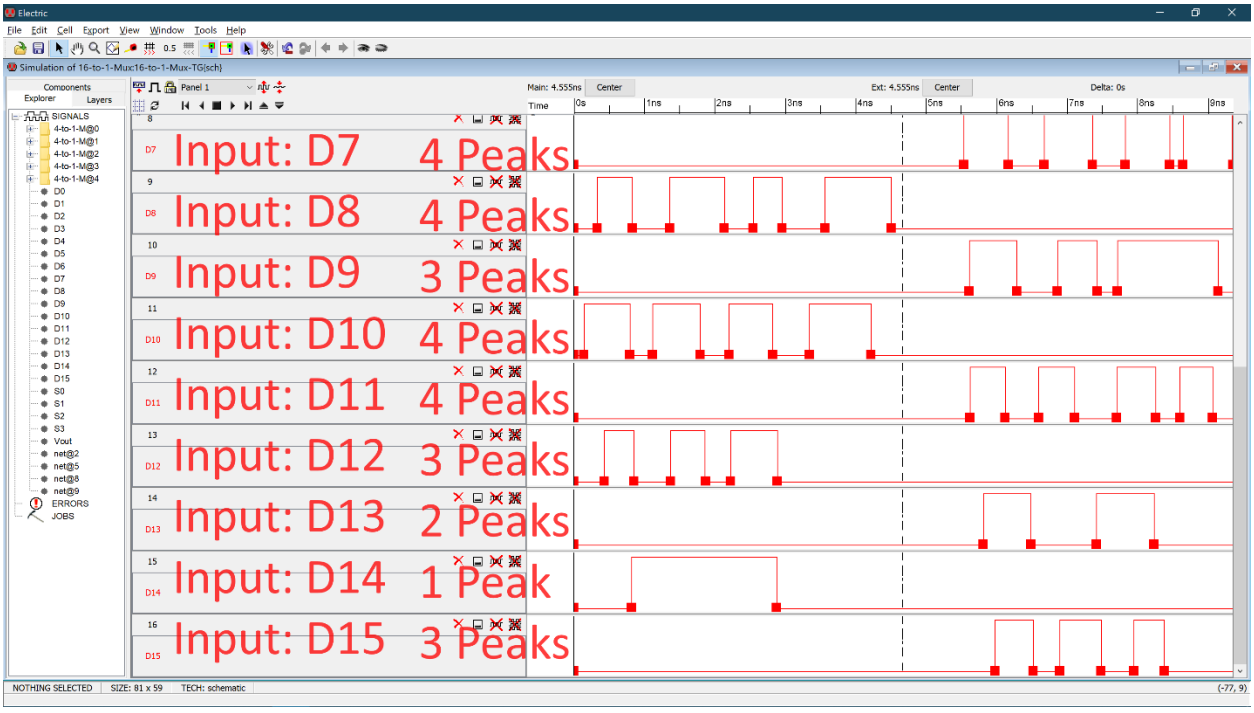

Figure 24.2: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer

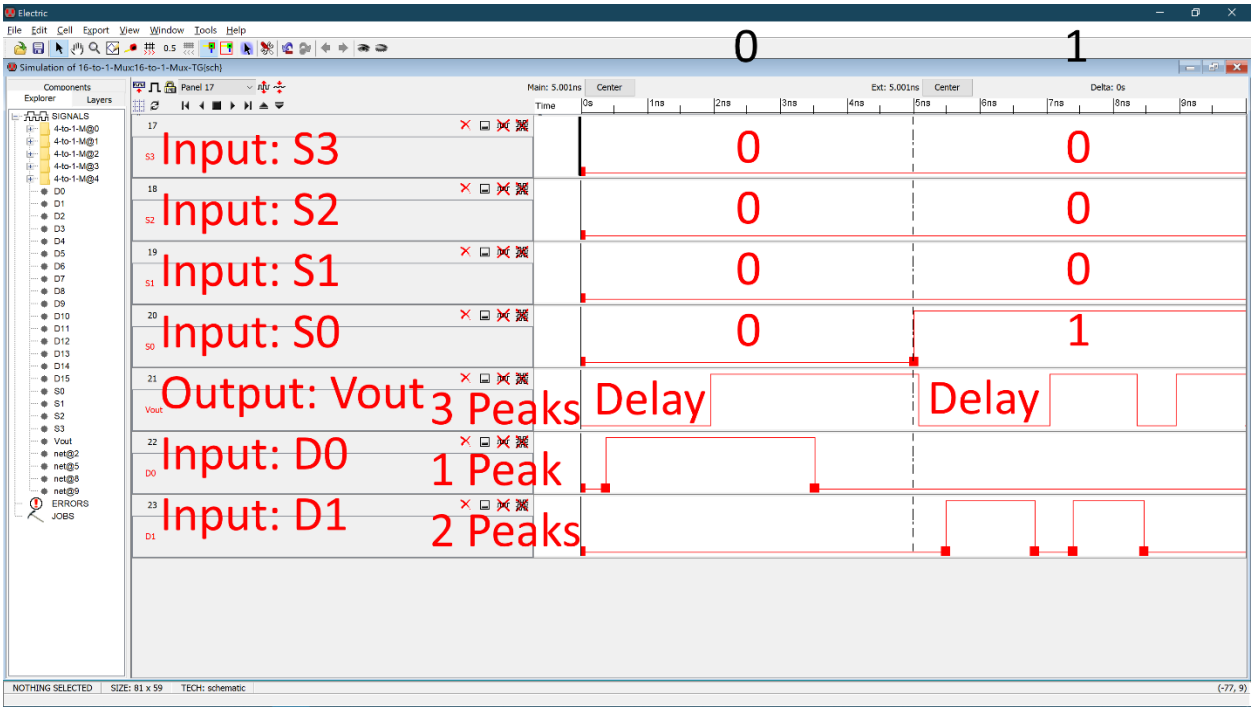

Figure 24.3: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 0 and 1)

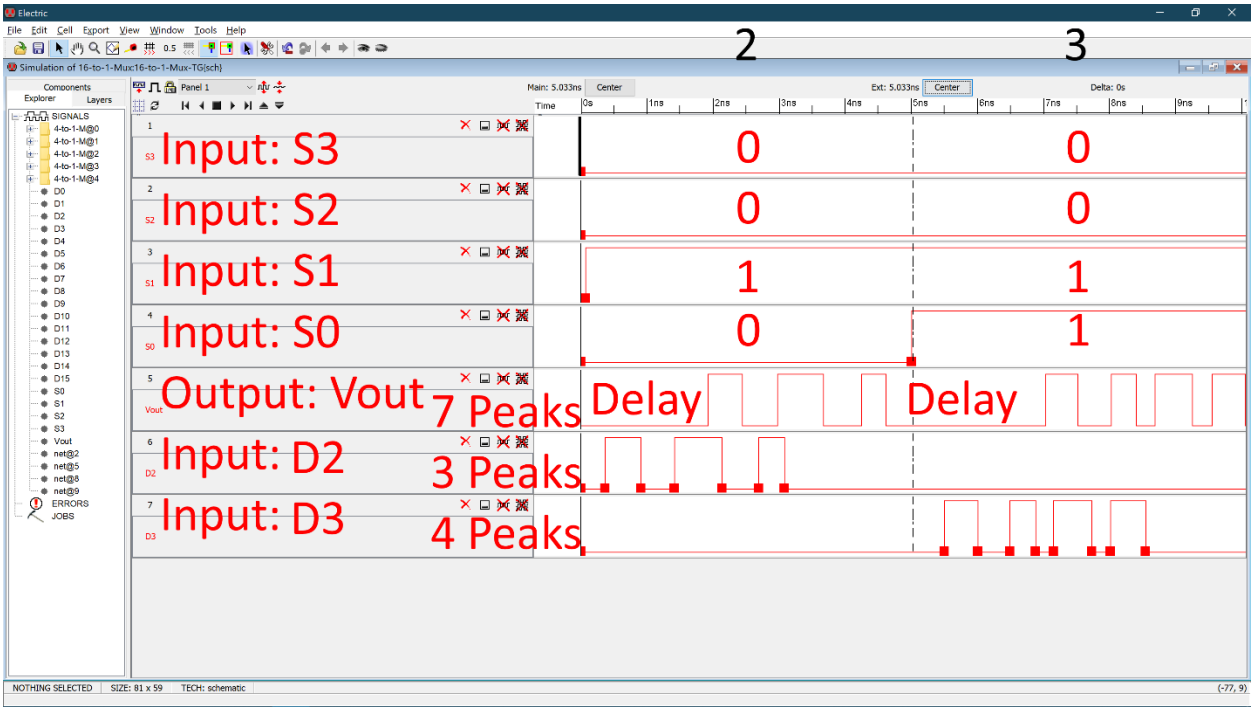

Figure 24.4: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 2 and 3)

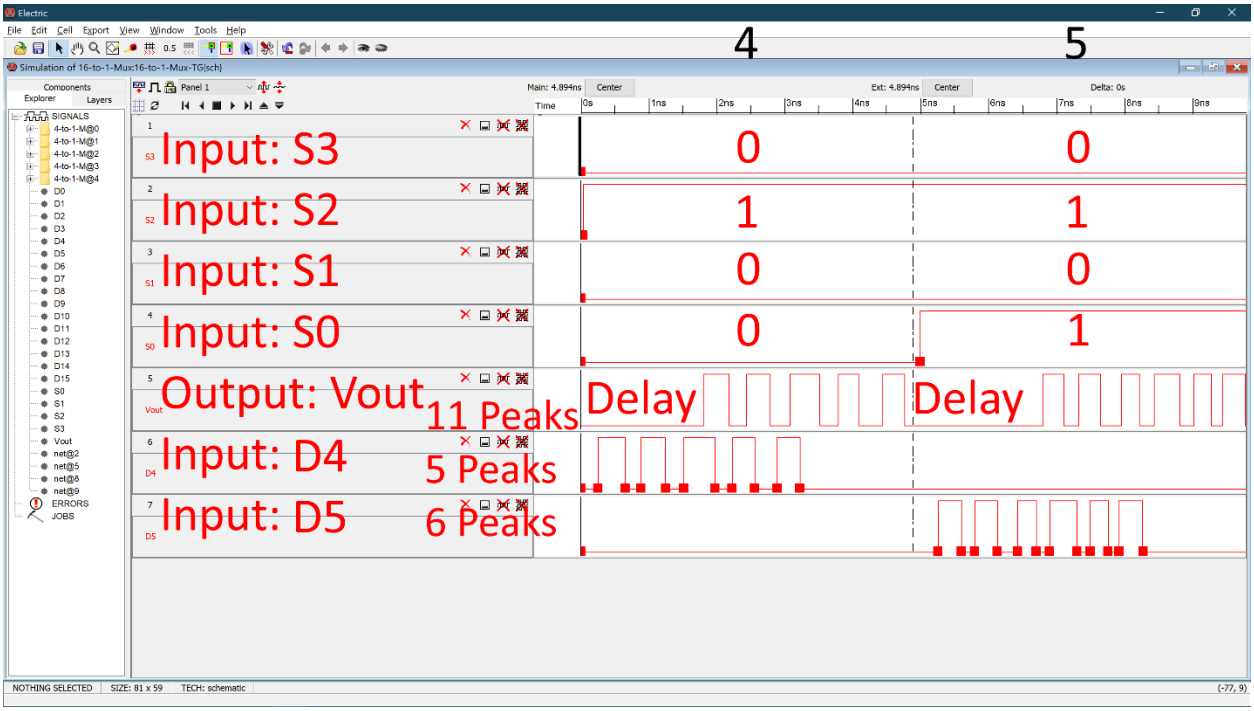

Figure 24.5: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 4 and 5)

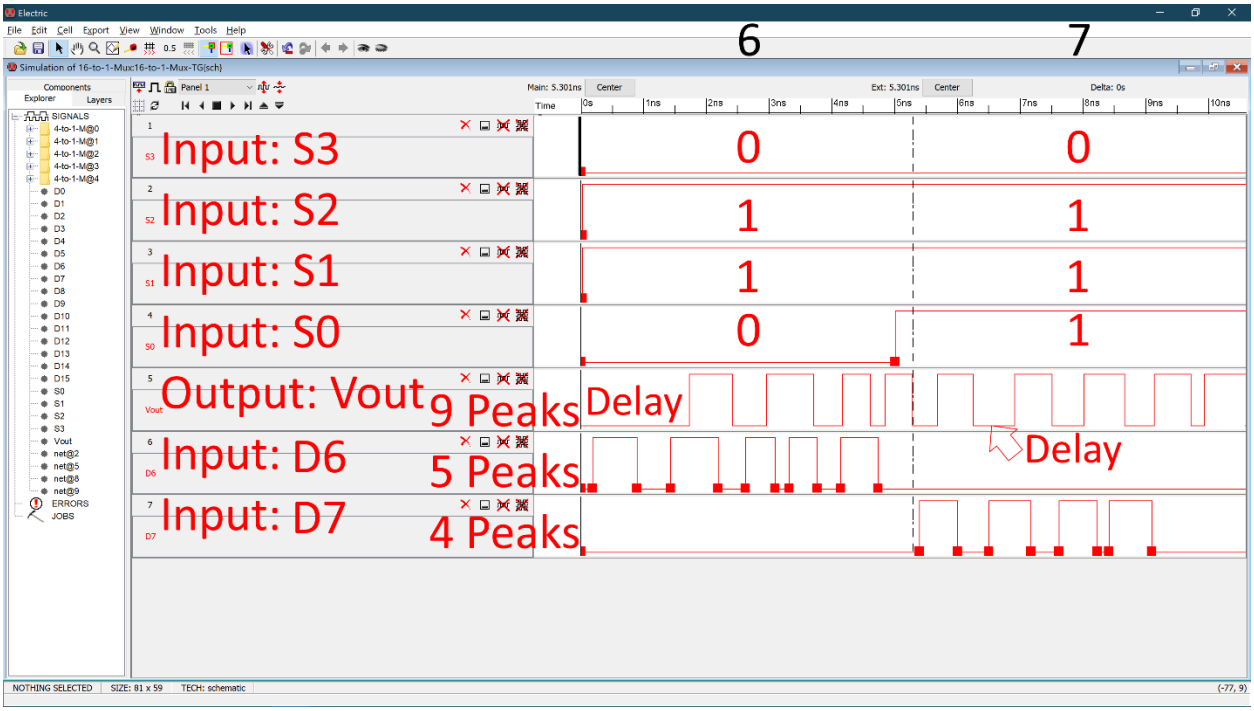

Figure 24.6: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 6 and 7)

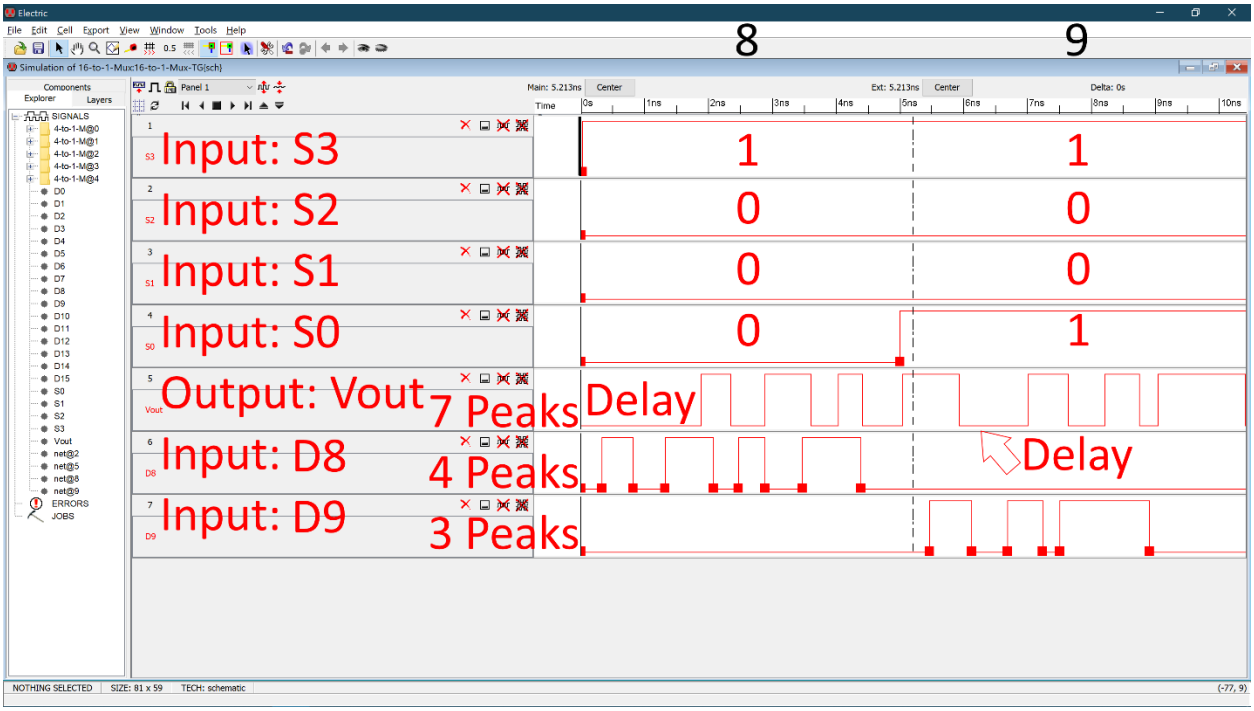

Figure 24.7: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 8 and 9)

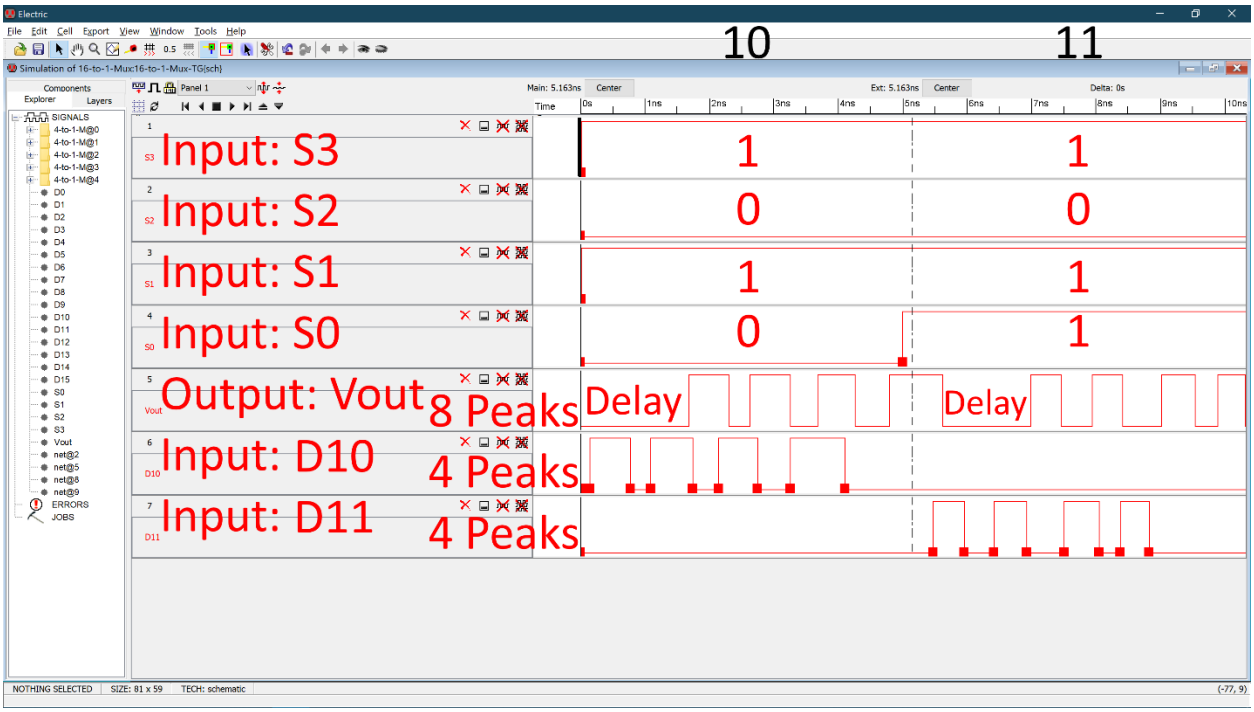

Figure 24.8: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 10 and 11)

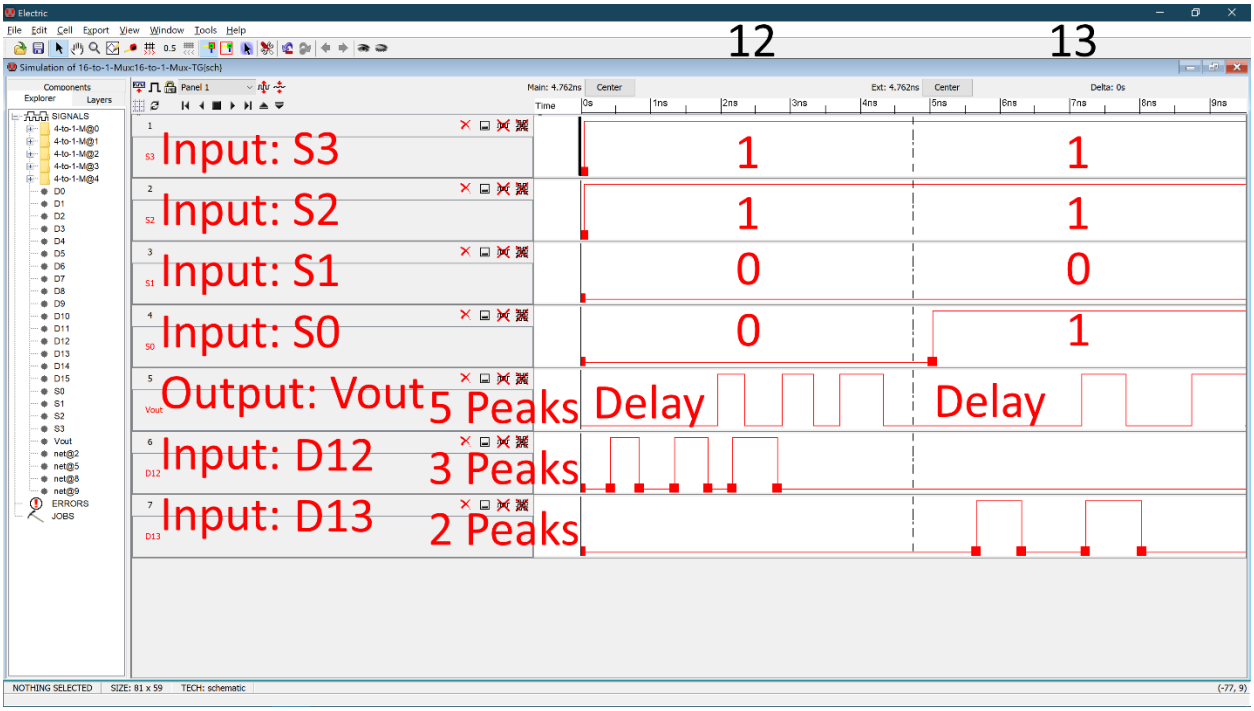

Figure 24.9: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 12 and 13)

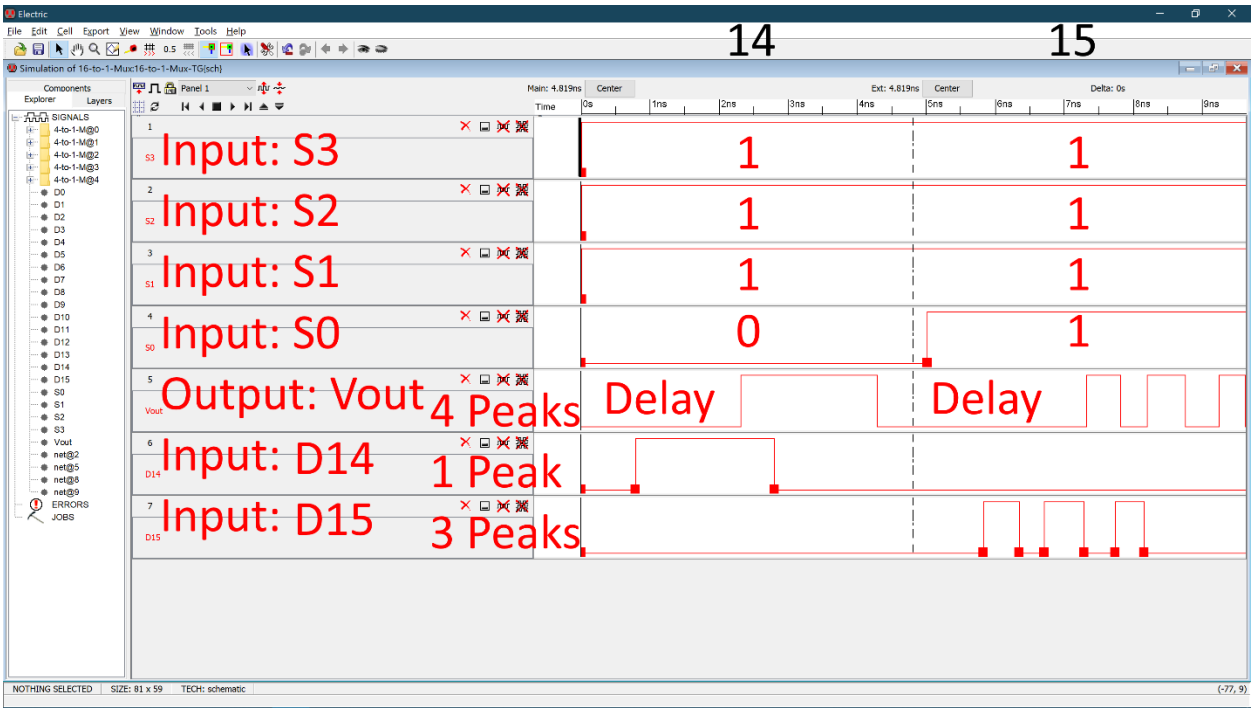

Figure 24.10: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 14 and 15)

Section 5.2: Layout:

For the layout, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the selectors and counting the peaks for the one that's selected and comparing it with the output.

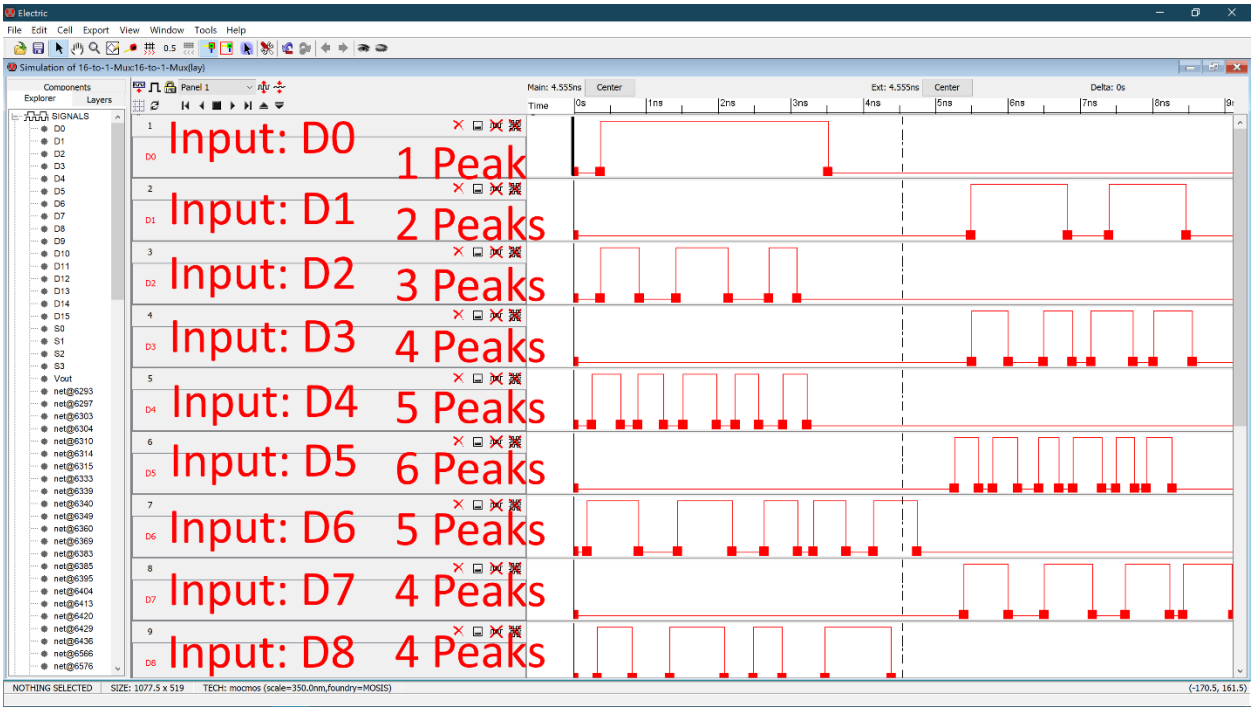

Figure 25.1: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer

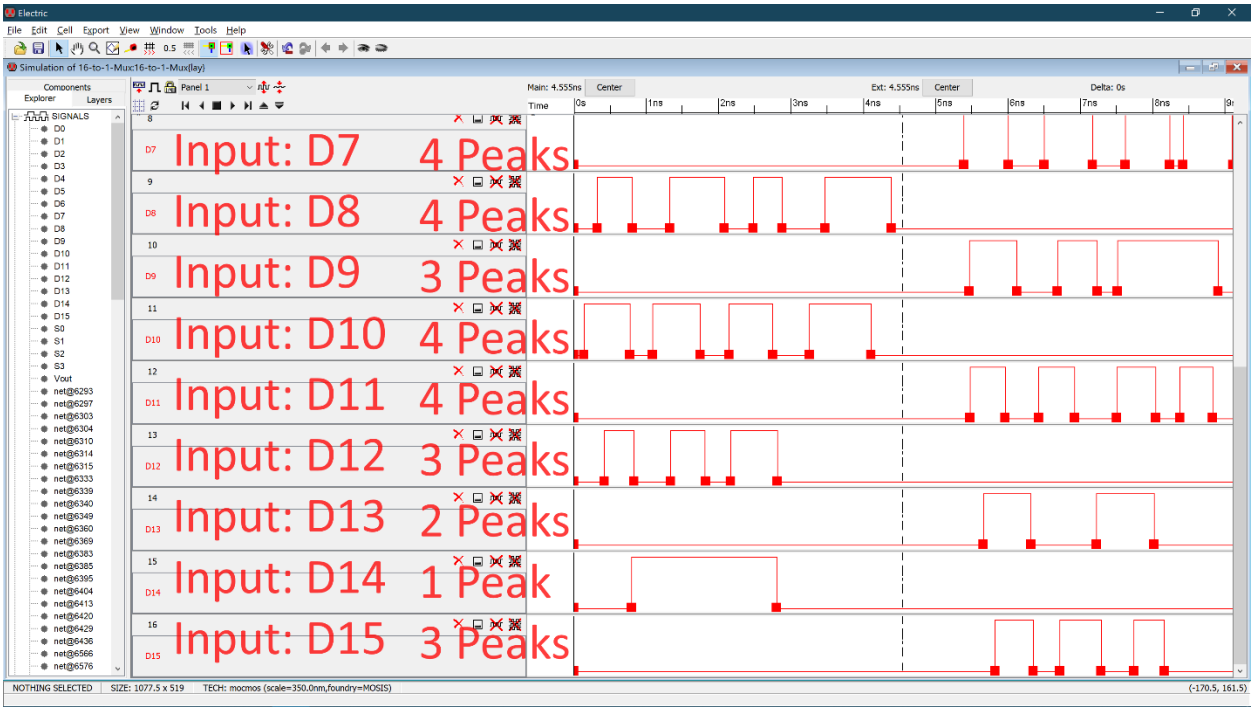

Figure 25.2: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer

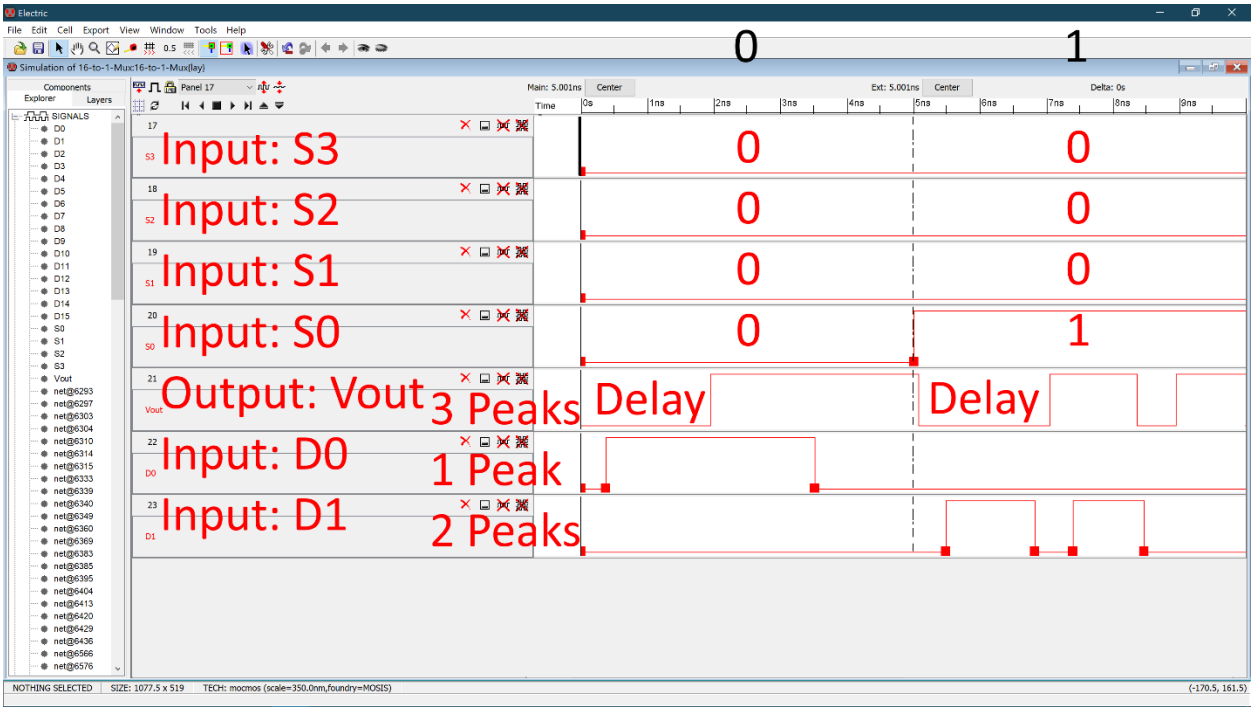

Figure 25.3: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 0 and 1)

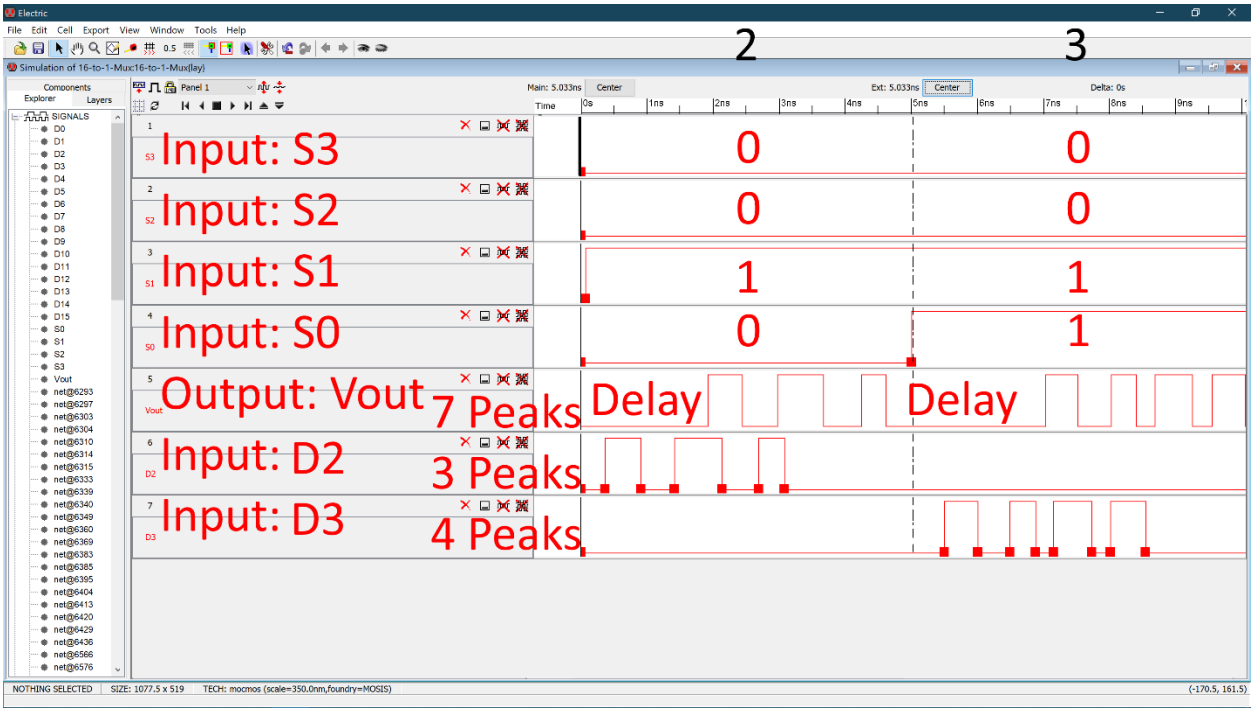

Figure 25.4: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 2 and 3)

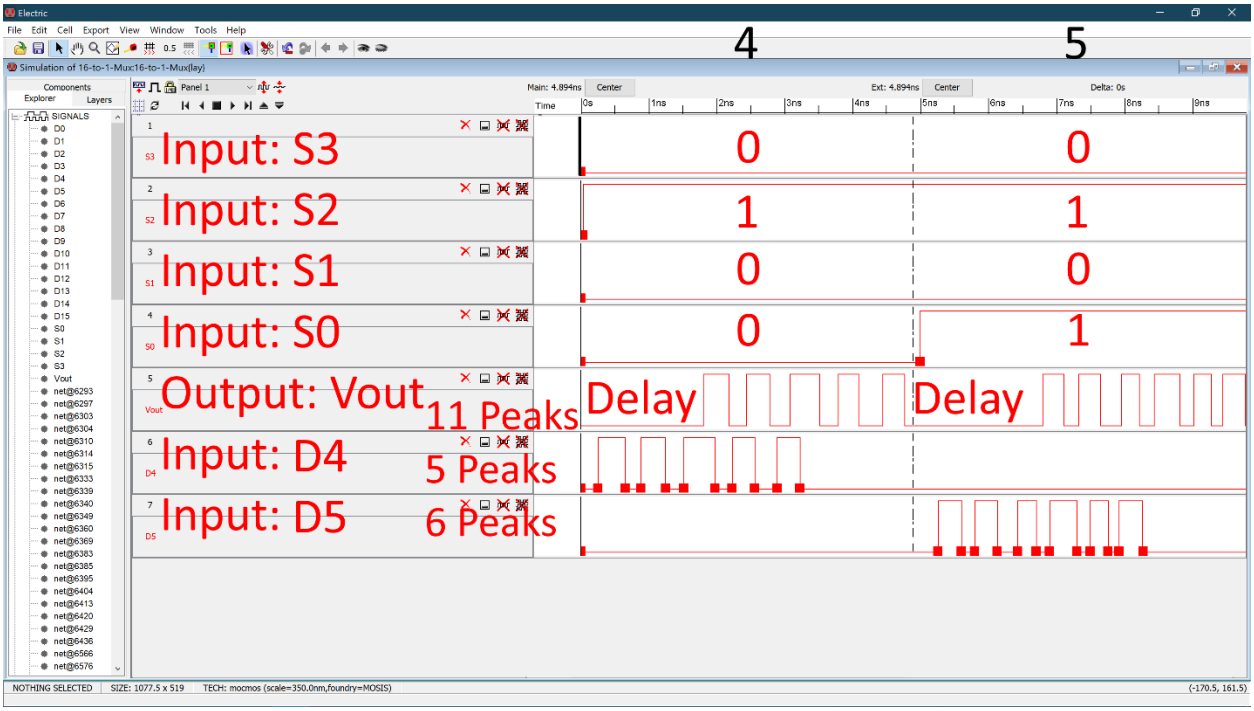

Figure 25.5: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 4 and 5)

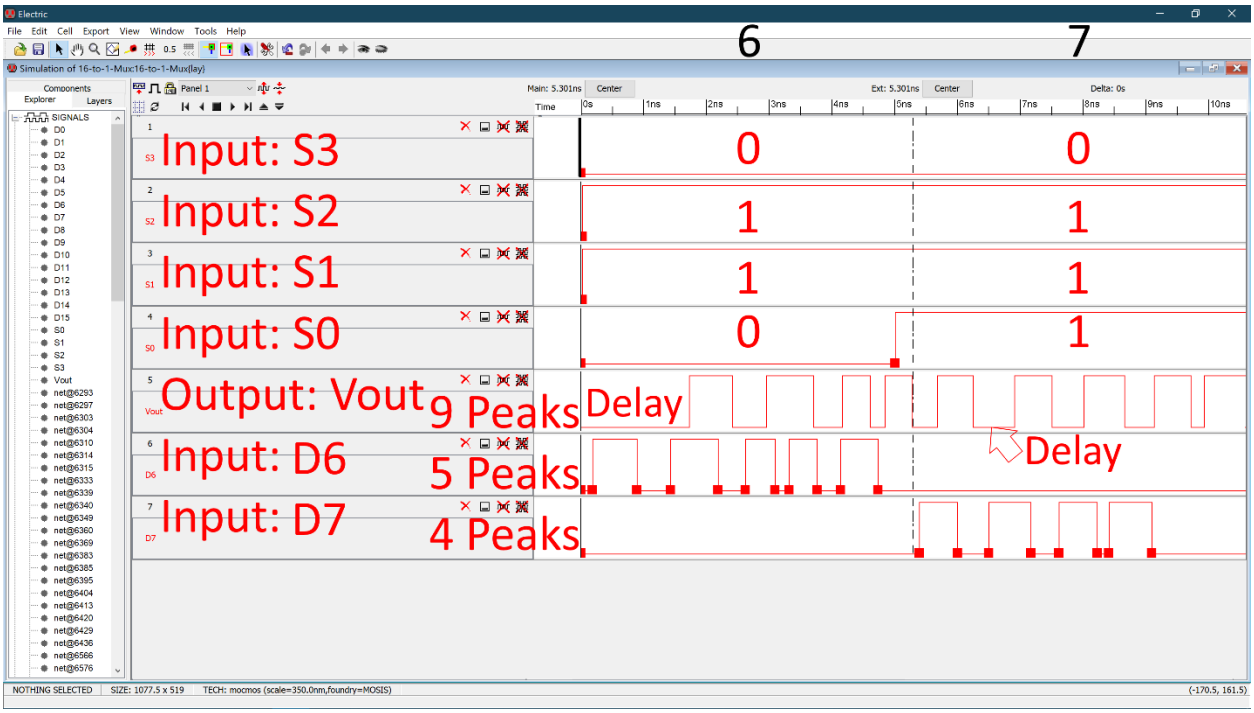

Figure 25.6: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 6 and 7)

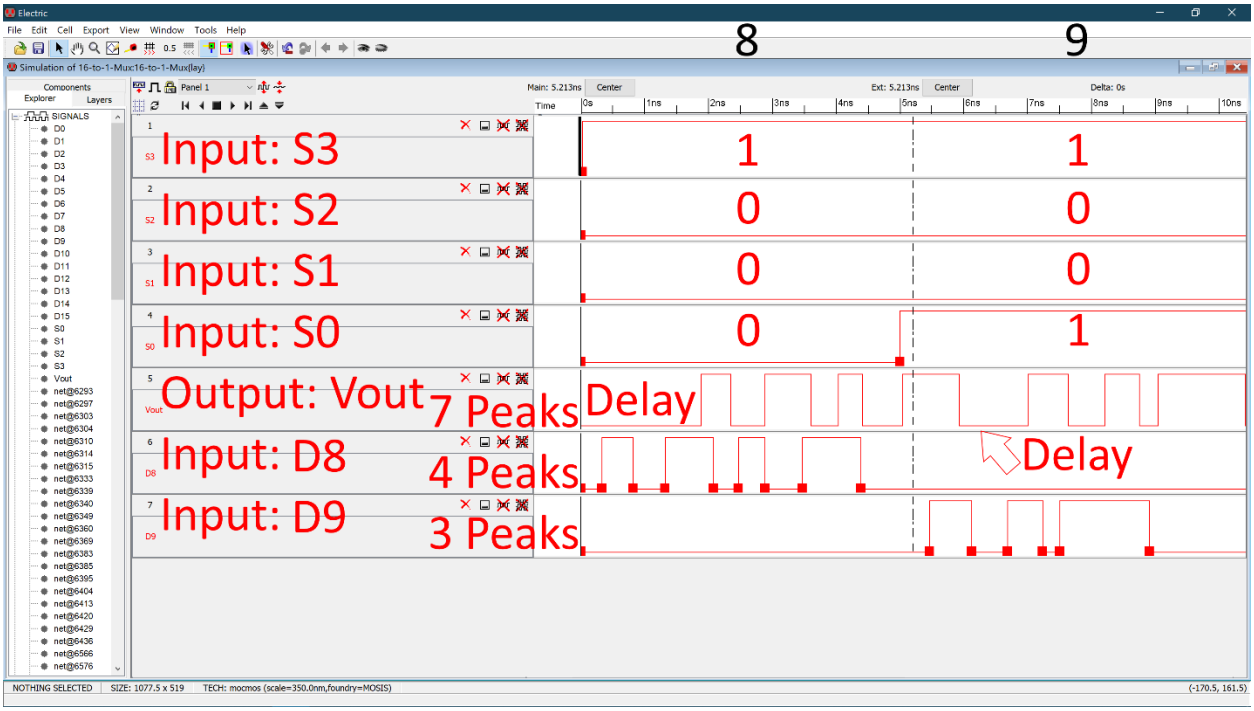

Figure 25.7: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 8 and 9)

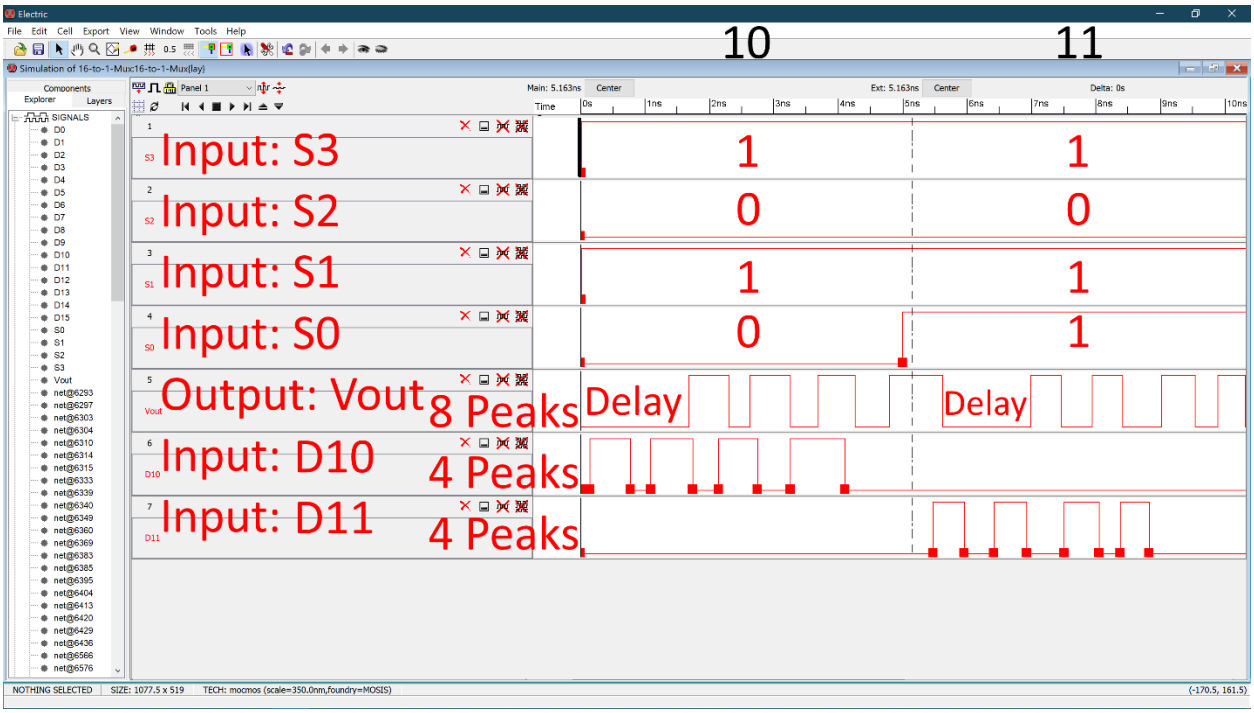

Figure 25.8: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 10 and 11)

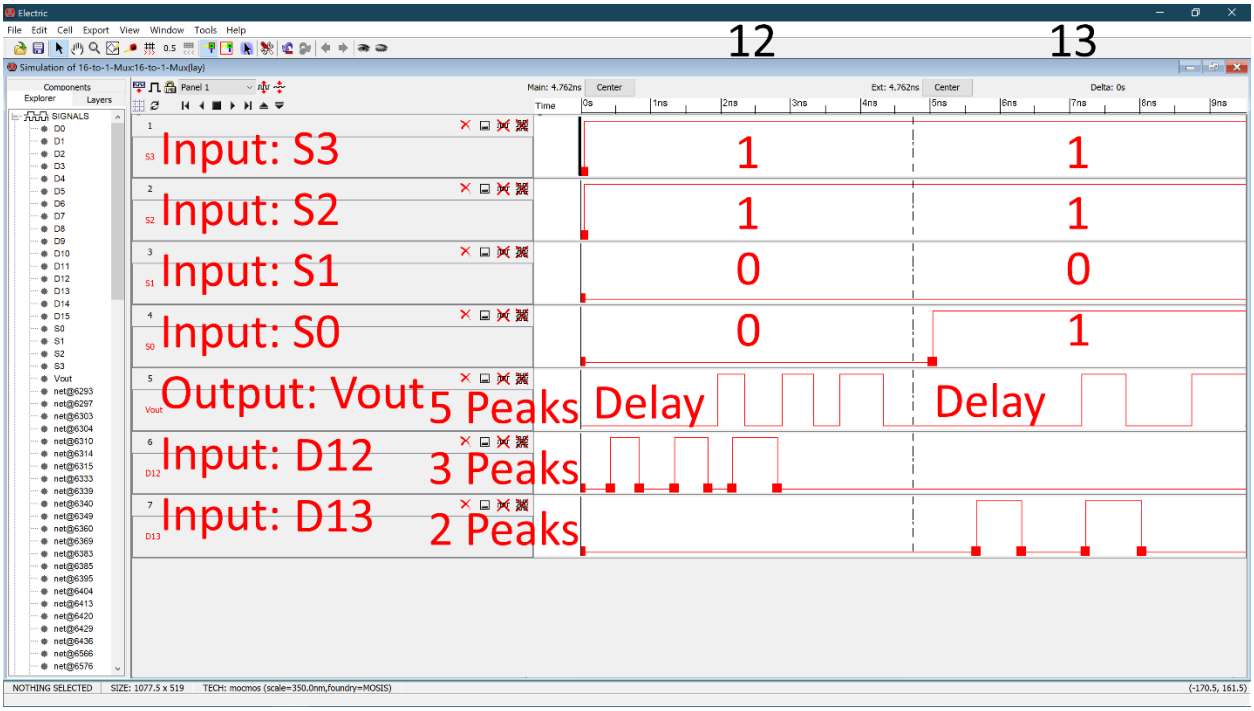

Figure 25.9: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 12 and 13)

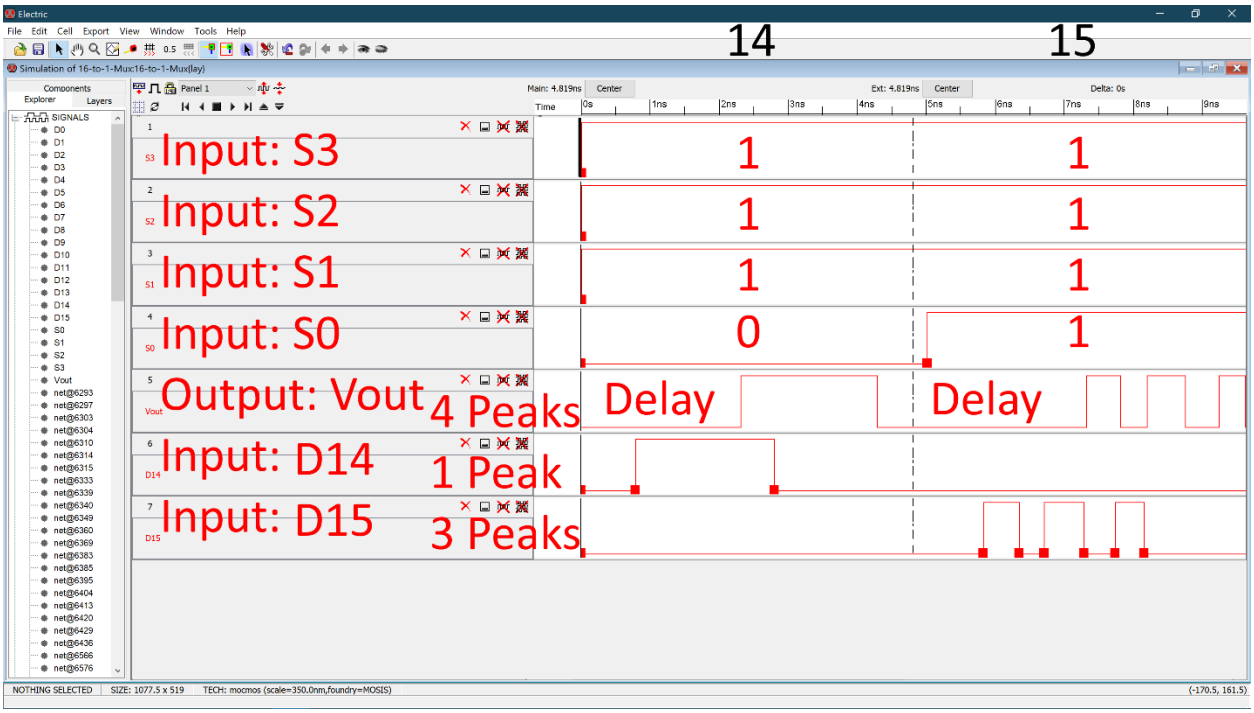

Figure 25.10: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 14 and 15)

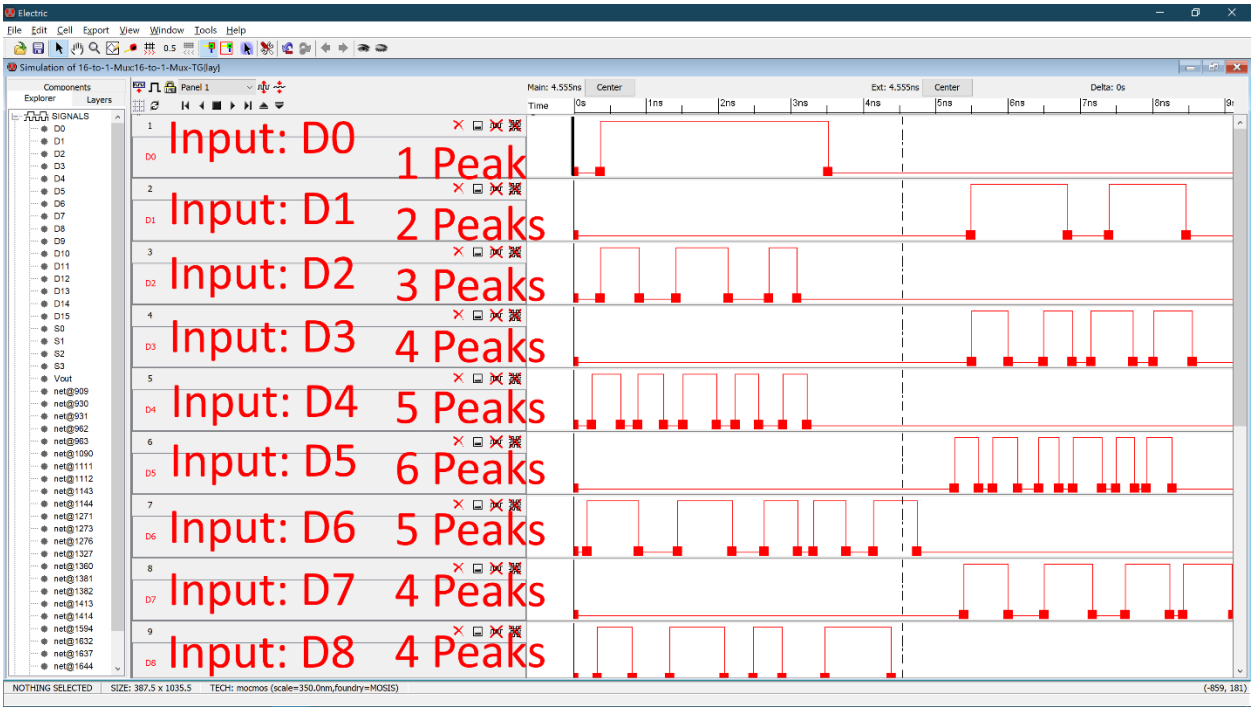

Figure 26.1: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer

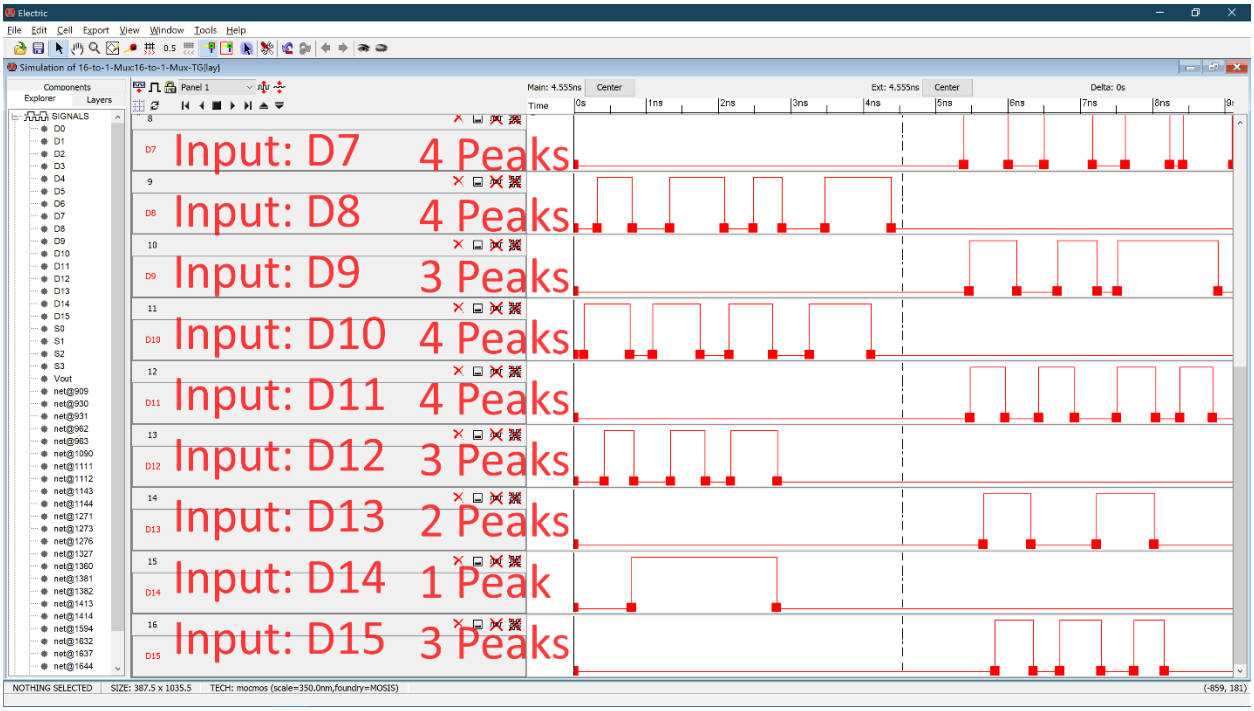

Figure 26.2: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer

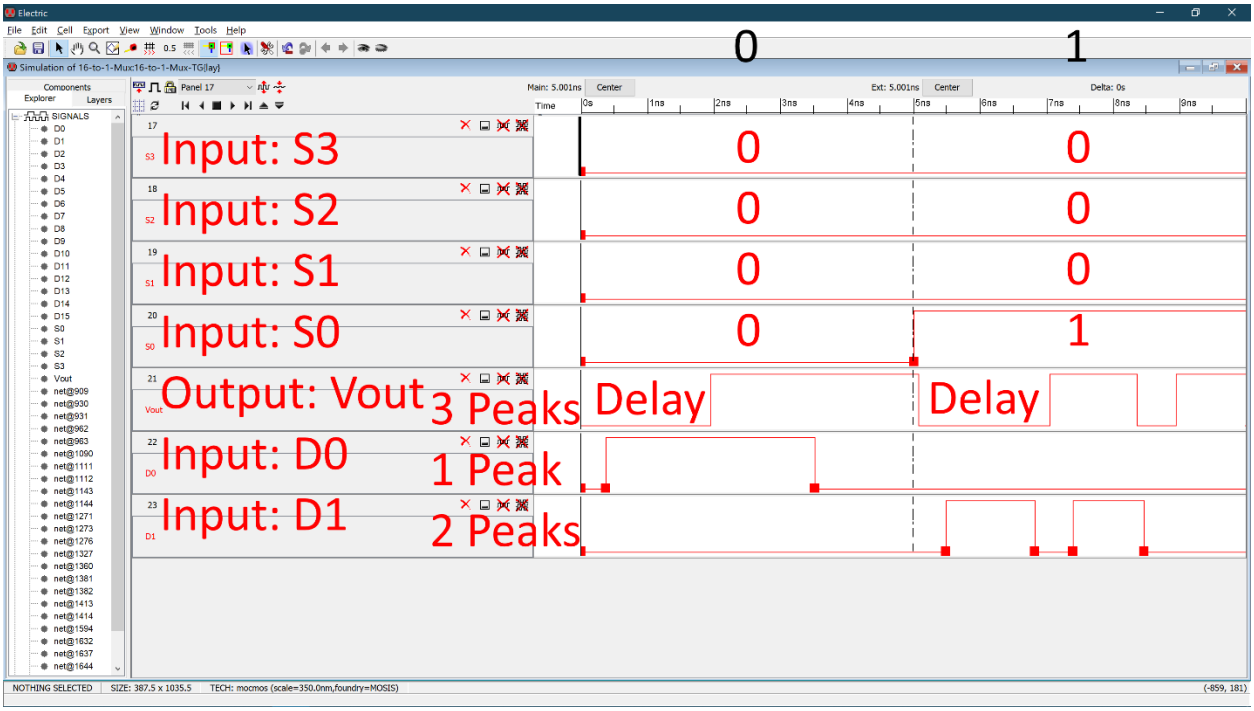

Figure 26.3: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 0 and 1)

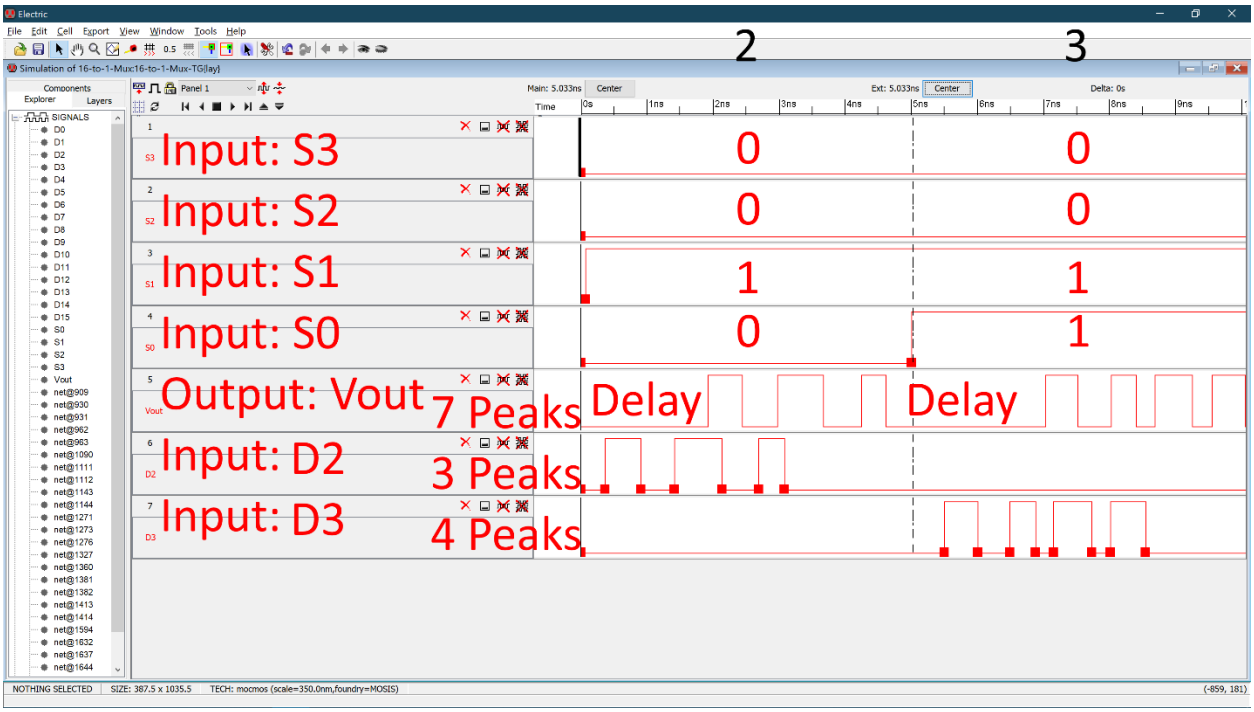

Figure 26.4: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 2 and 3)

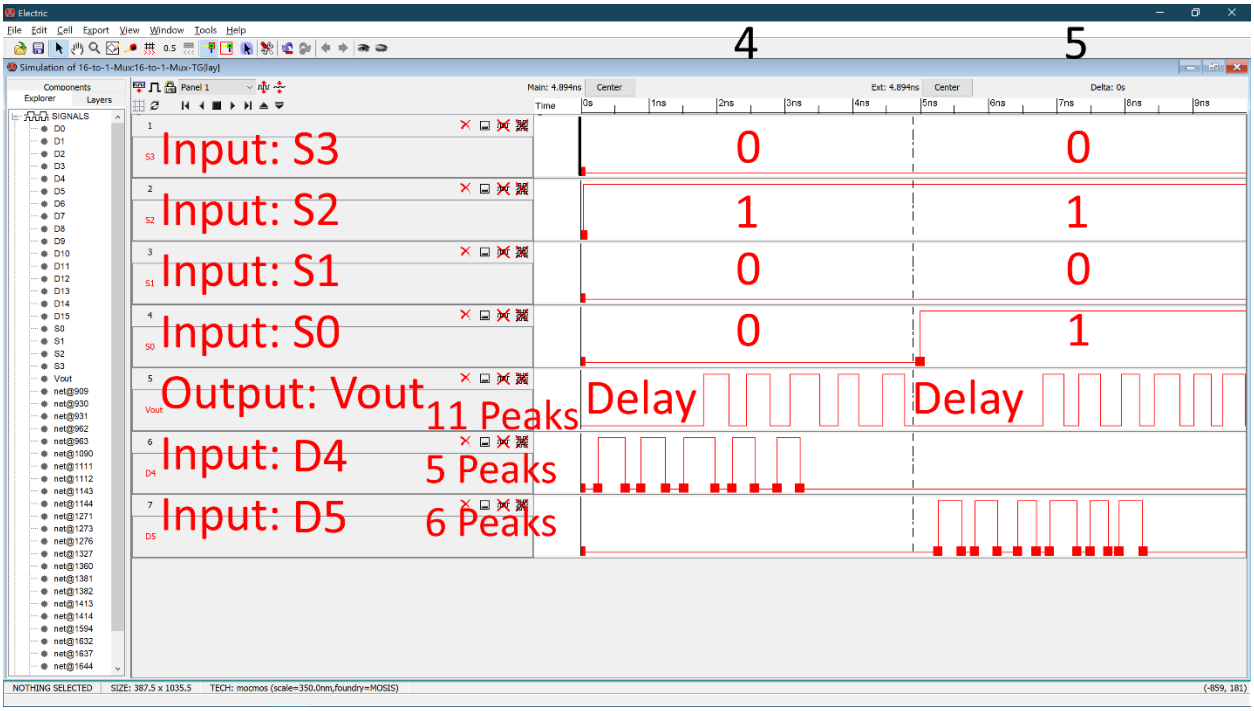

Figure 26.5: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 4 and 5)

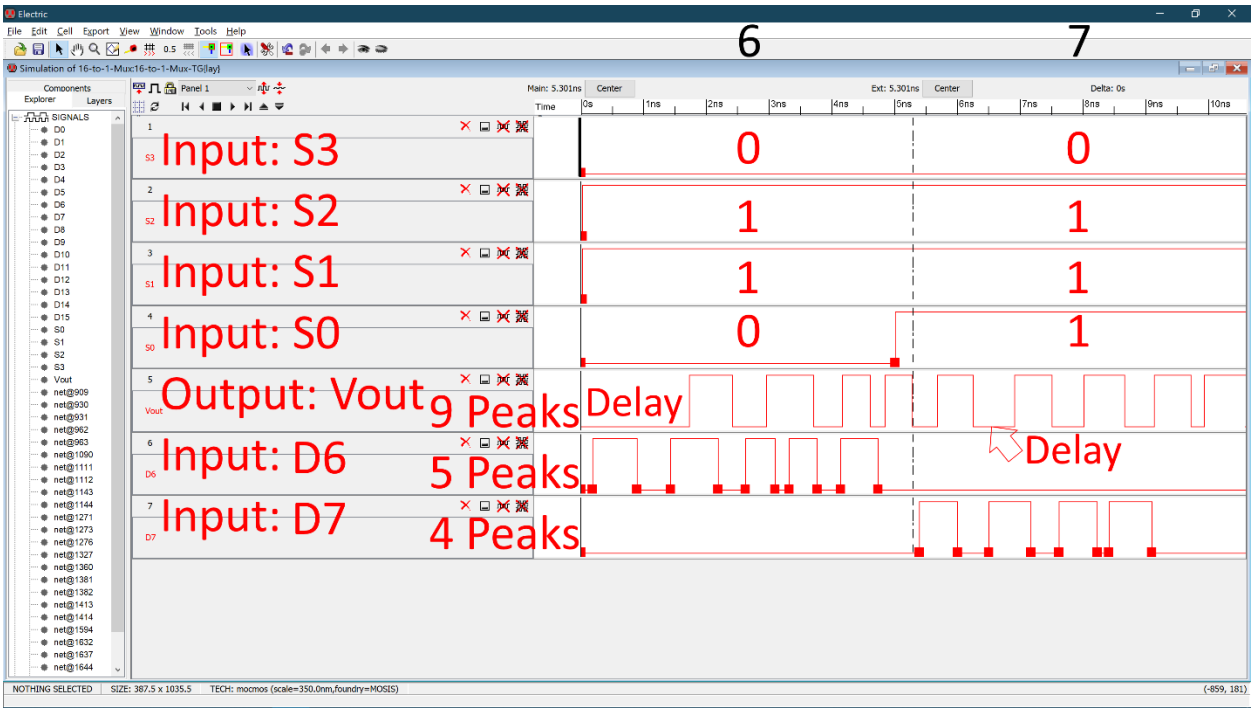

Figure 26.6: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 6 and 7)

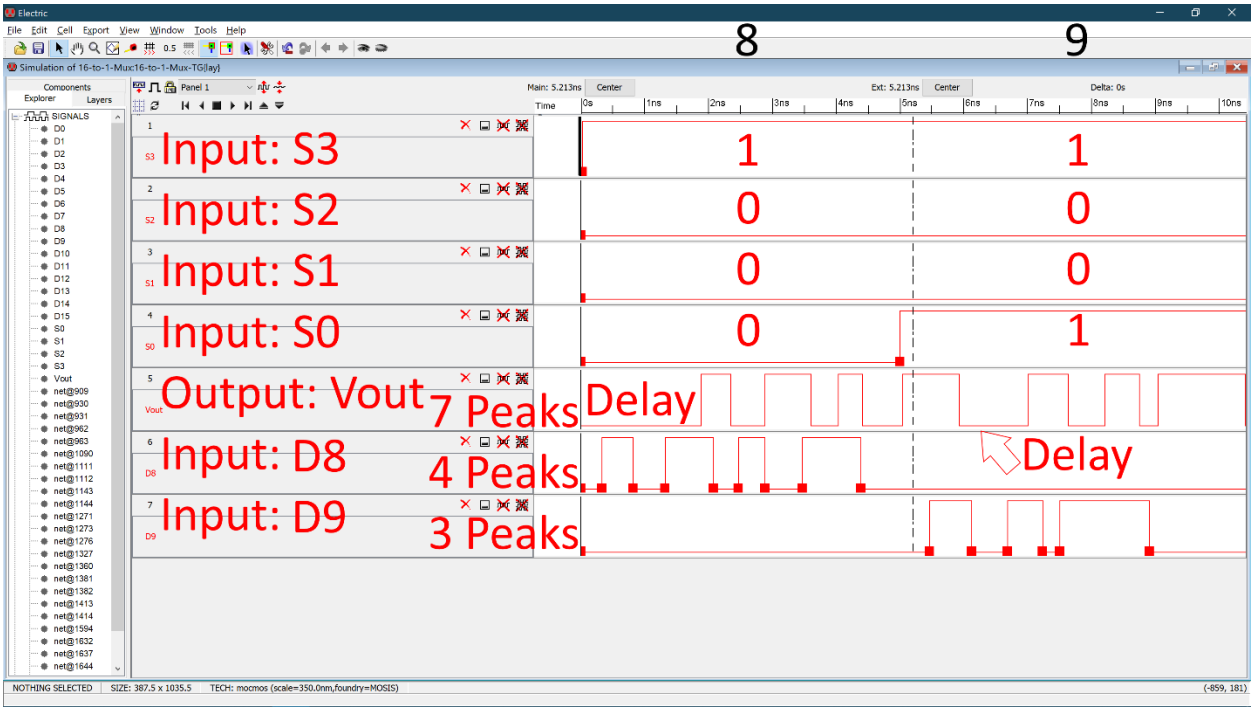

Figure 26.7: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 8 and 9)

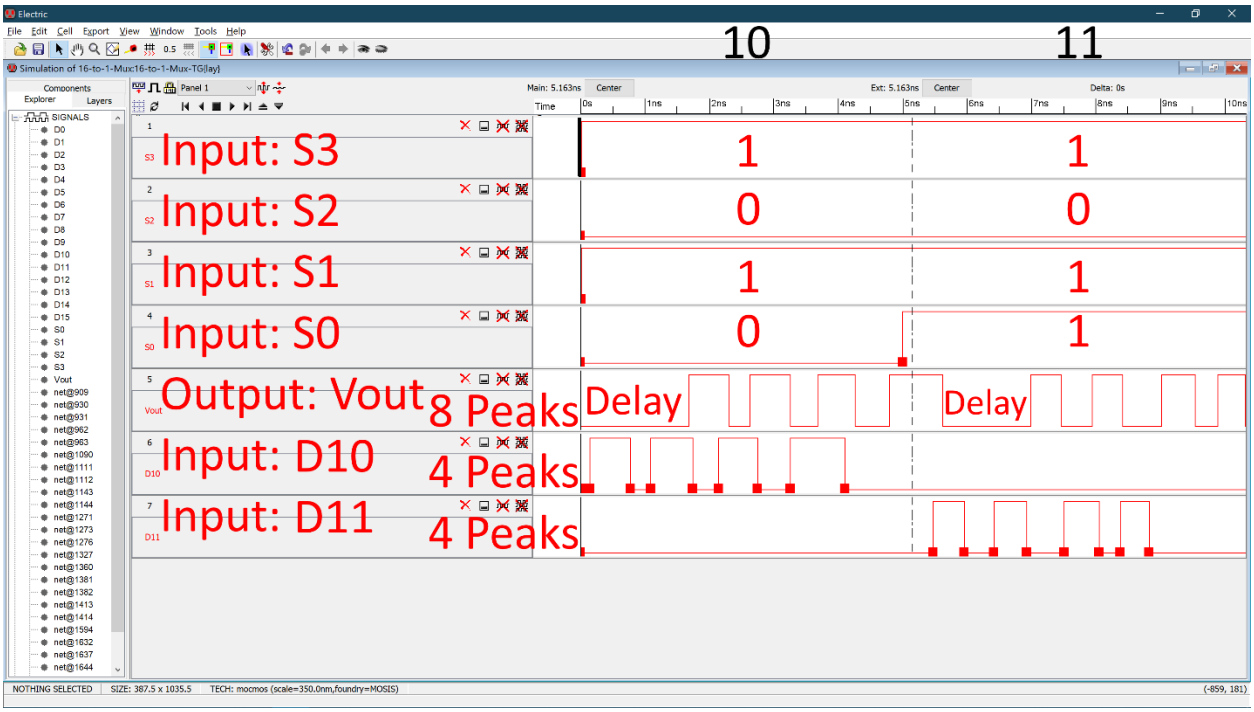

Figure 26.8: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 10 and 11)

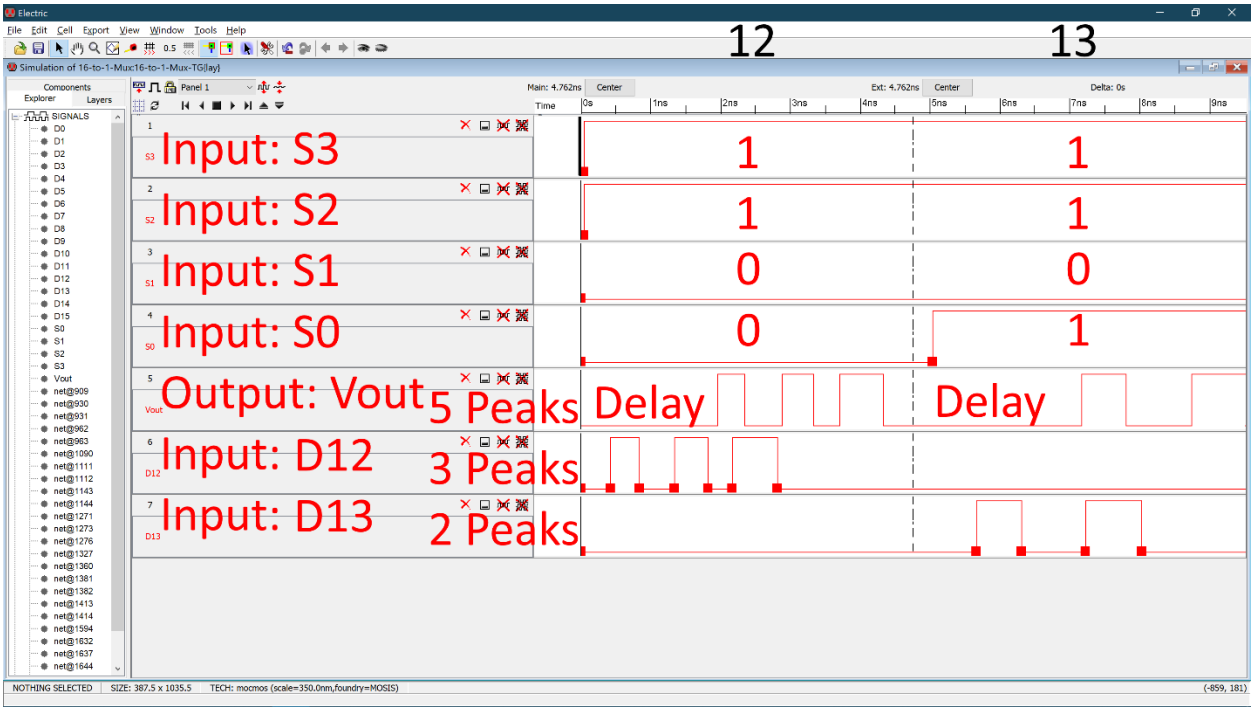

Figure 26.9: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 12 and 13)

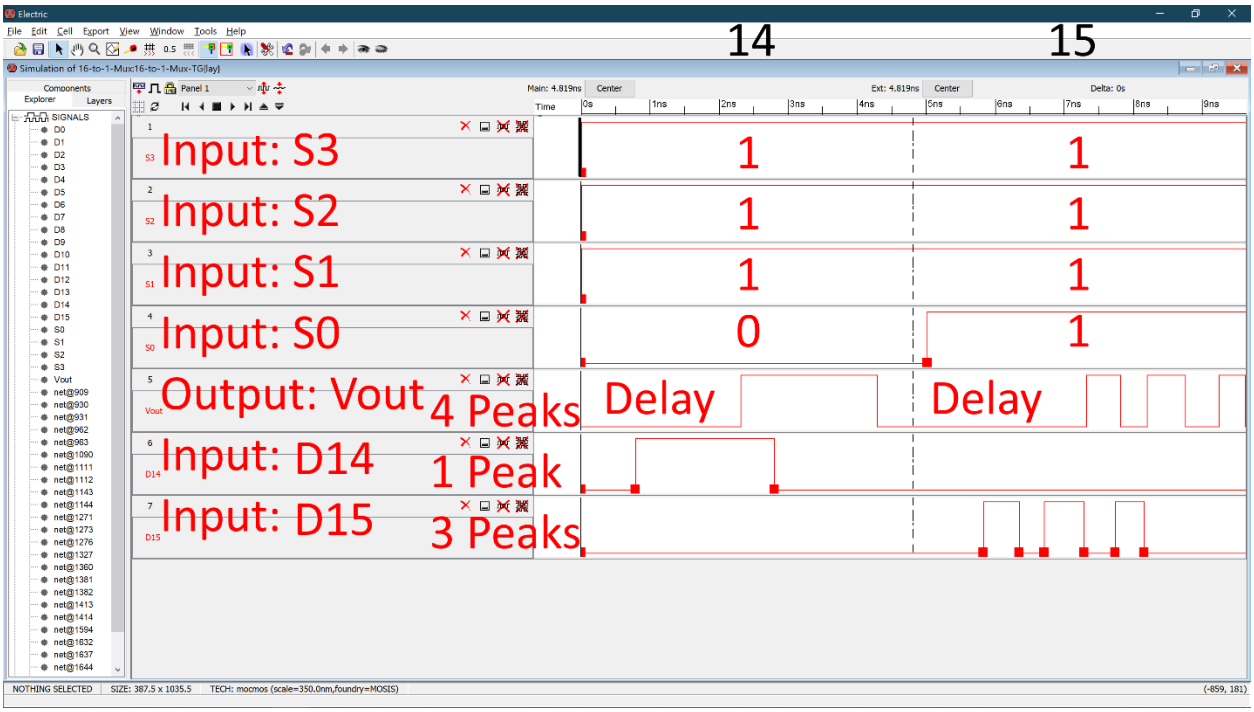

Figure 26.10: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 14 and 15)

Section 5.3: Comparison:

For IRSIM, by comparing Figure 23 (Conventional Schematic), Figure 24 (Transmission Gate Schematic), Figure 25 (Conventional Layout), and Figure 26 (Transmission Gate Layout) with each other, the way the output reacted given the certain inputs appears to be the same. In addition, with the inputs we gave, it gave us the appropriate outputs that we were looking for, so it confirms that our design is correct. The outputs that we were looking from could be seen by using the truth table on Table 1. The only noticeable difference between the figures would be the propagation delay, which could be seen on Table 6. Depending on the which design, each has its own different propagation delay.

In conclusion, IRSIM shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time, and propagation delay. The differences can be viewed on Table 6, which has a summary of the measurements.

Section 6: LTSPICE Code and Parasitic Extractions:

The Spice Code that we wrote is shown on Figure 27. It provides certain values to the inputs so that it'll be able to produce a certain output. The computations that we tested set each input (D0-D15) high for 50 nanoseconds at different times, then back to low; in other words, 100 nanoseconds period, with rise time and fall time of 5 nanoseconds and 50% duty cycle. Each of the inputs were high at different times so they wouldn't be able to relate to each other. After that, we set tested all the computations for the selector (S0-S3), starting from 0 to 15. This way, it'll be able to output each individual input and show a wavelike output.

We ran LTSPICE on the conventional 16-to-1 Multiplexer Schematic, conventional 16-to-1 Multiplexer Layout, transmission gate 16-to-1 Multiplexer Schematic, and transmission gate 16-to-1 Multiplexer Layout and it generated a code underneath it. A sample of the Spice Deck and Parasitic Extractions that came from those designs are shown from Figure 28 to Figure 35.

```
VDD VDD 0 DC 3.3
VGND GND 0 DC 0
Vin2 D0 0 PULSE (0 3.3 0n 5n 5n 50n 1600n)
Vin3 D1 0 PULSE (0 3.3 100n 5n 5n 50n 1600n)
Vin4 D2 0 PULSE (0 3.3 200n 5n 5n 50n 1600n)
Vin5 D3 0 PULSE (0 3.3 300n 5n 5n 50n 1600n)
Vin6 D4 0 PULSE (0 3.3 400n 5n 5n 50n 1600n)
Vin7 D5 0 PULSE (0 3.3 500n 5n 5n 50n 1600n)
Vin8 D6 0 PULSE (0 3.3 600n 5n 5n 50n 1600n)
Vin9 D7 0 PULSE (0 3.3 700n 5n 5n 50n 1600n)
Vin10 D8 0 PULSE (0 3.3 800n 5n 5n 50n 1600n)
Vin11 D9 0 PULSE (0 3.3 900n 5n 5n 50n 1600n)
Vin12 D10 0 PULSE (0 3.3 1000n 5n 5n 50n 1600n)
Vin13 D11 0 PULSE (0 3.3 1100n 5n 5n 50n 1600n)
Vin14 D12 0 PULSE (0 3.3 1200n 5n 5n 50n 1600n)
Vin15 D13 0 PULSE (0 3.3 1300n 5n 5n 50n 1600n)
Vin16 D14 0 PULSE (0 3.3 1400n 5n 5n 50n 1600n)
Vin17 D15 0 PULSE (0 3.3 1500n 5n 5n 50n 1600n)
Vin18 S0 0 PULSE (0 3.3 100n 5n 5n 100n 200n)
Vin19 S1 0 PULSE (0 3.3 200n 5n 5n 200n 400n)
Vin20 S2 0 PULSE (0 3.3 400n 5n 5n 400n 800n)
Vin21 S3 0 PULSE (0 3.3 800n 5n 5n 800n 1600n)
.TRAN 0 1600n
.include C:\Users\kille\Desktop\Electric\C5_models.txt
```

Figure 27: Spice Code Written For LTSPICE

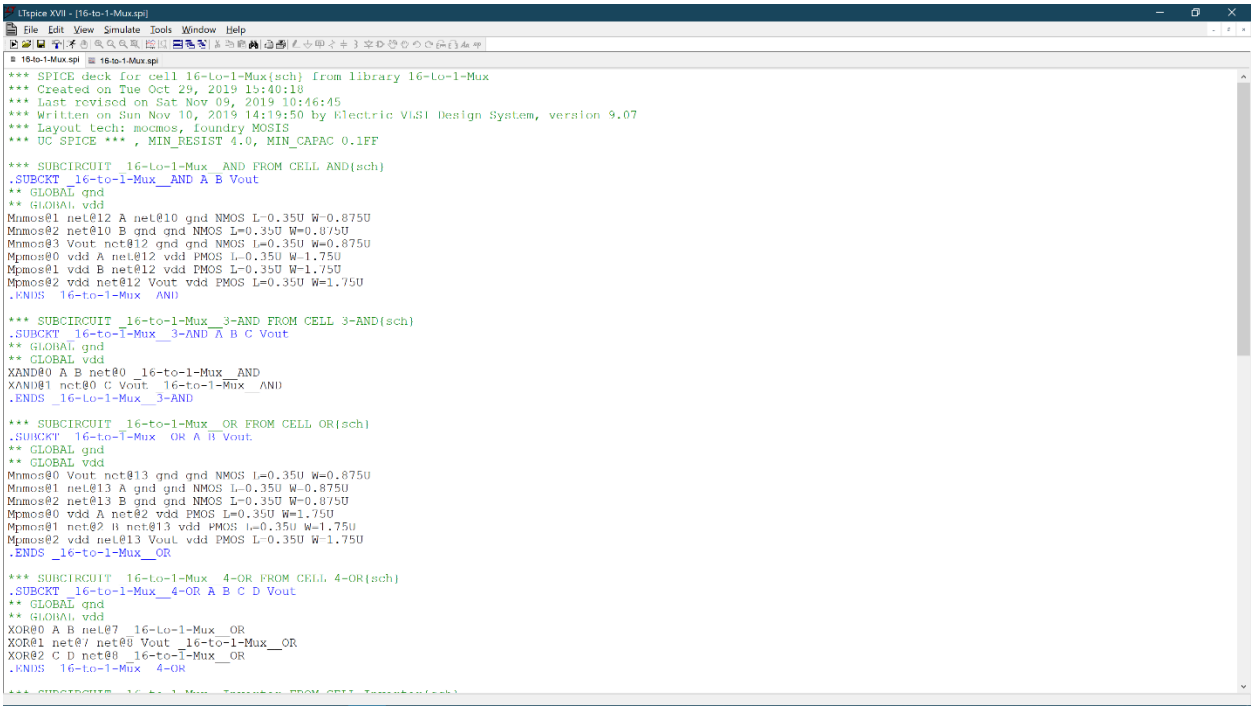

Figure 28: Generated Spice Deck of Conventional 16-to-1 Multiplexer Schematic

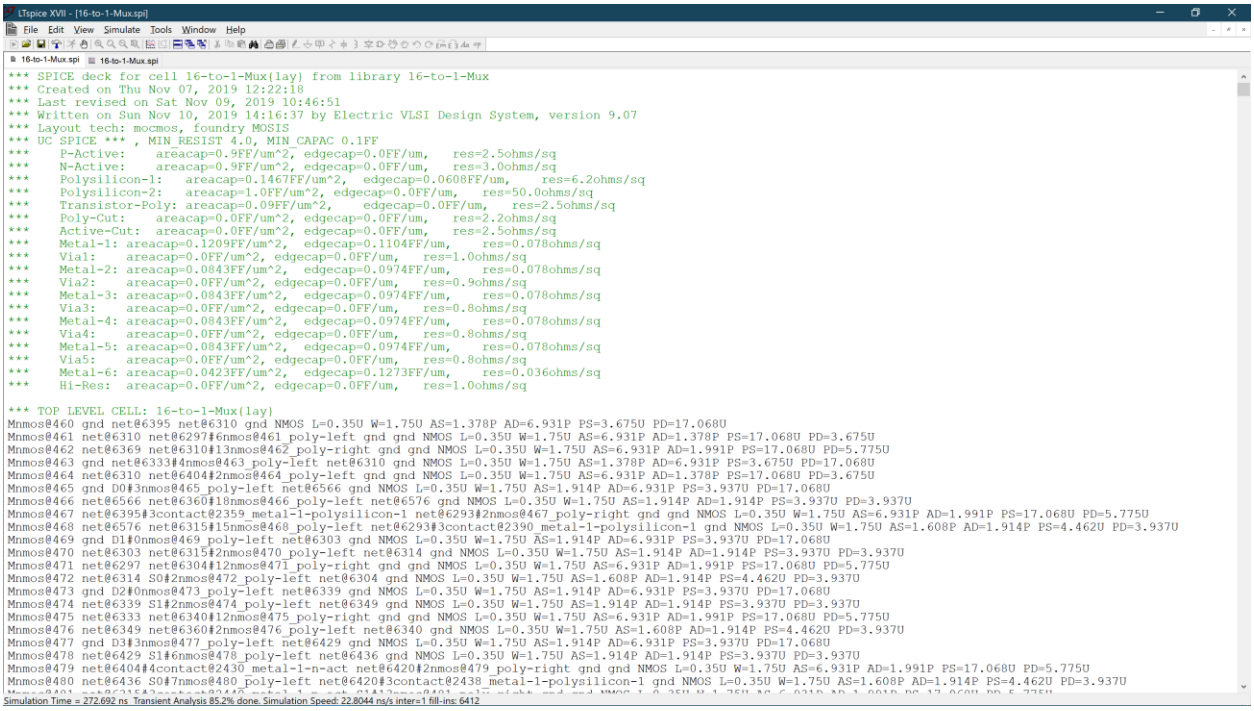

Figure 29: Generated Spice Deck of Conventional 16-to-1 Multiplexer Layout

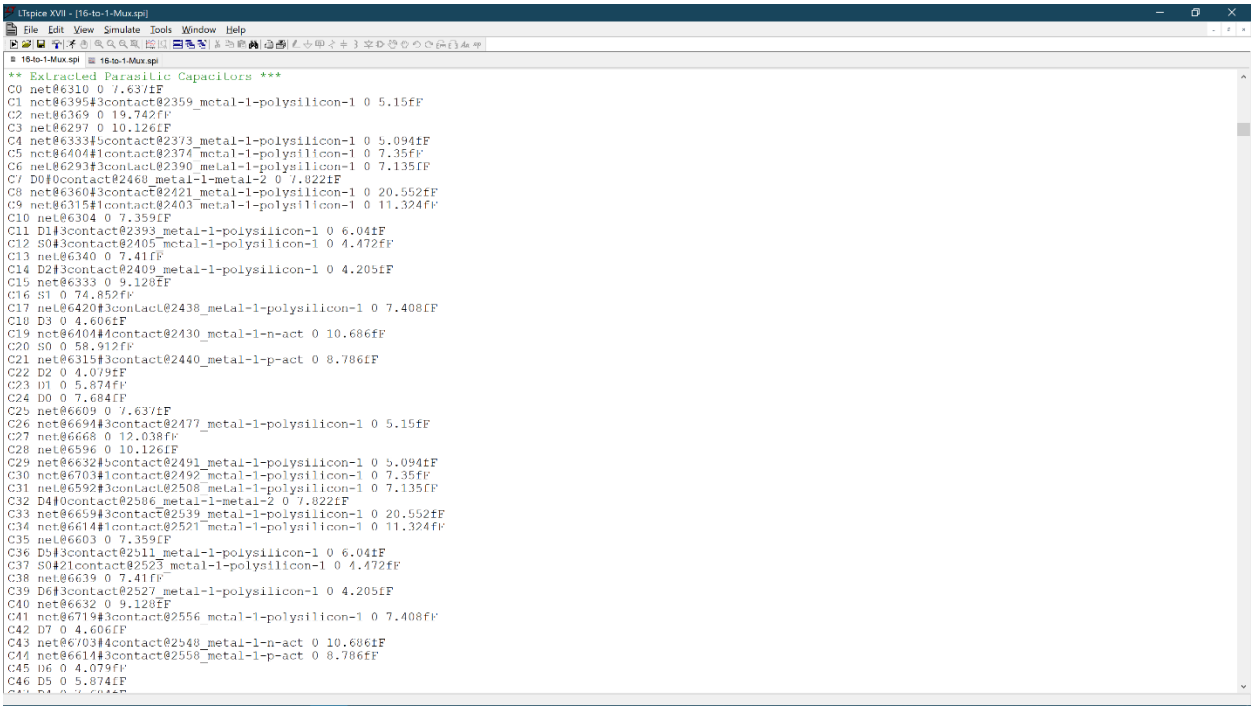

Figure 30: Extracted Parasitic Capacitors Sample of Conventional 16-to-1 Multiplexer Layout

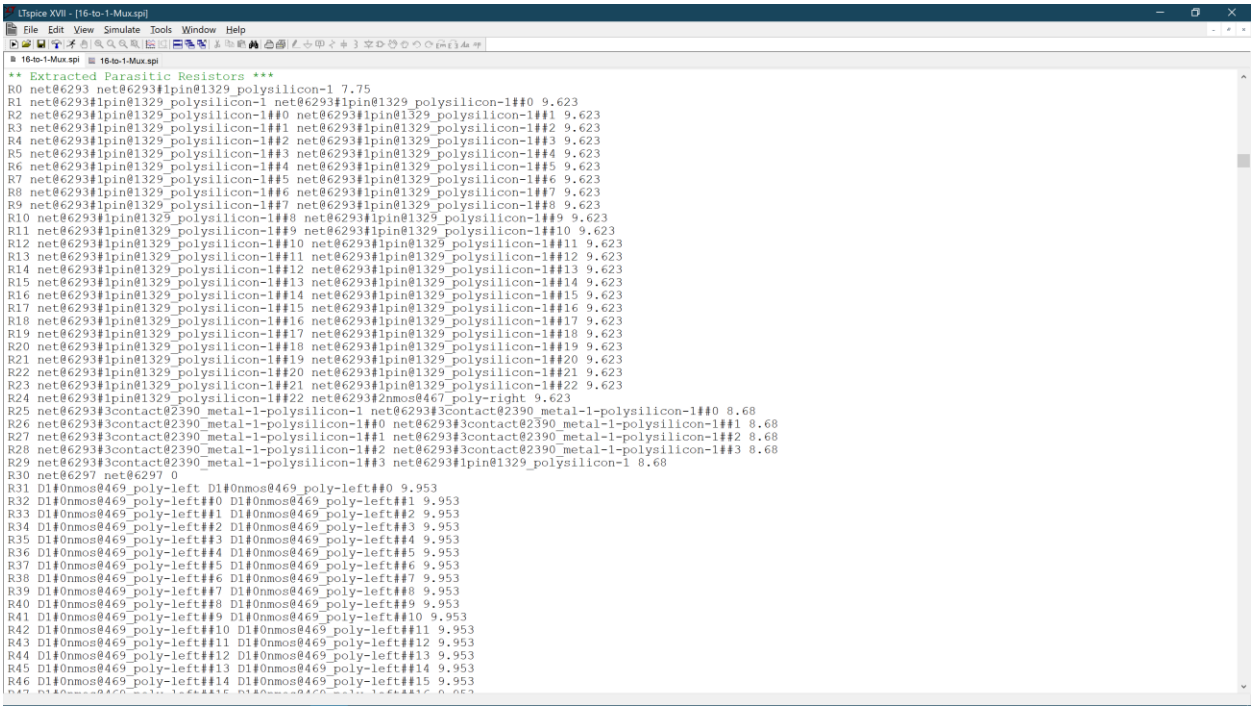

Figure 31: Extracted Parasitic Resistors Sample of Conventional 16-to-1 Multiplexer Layout

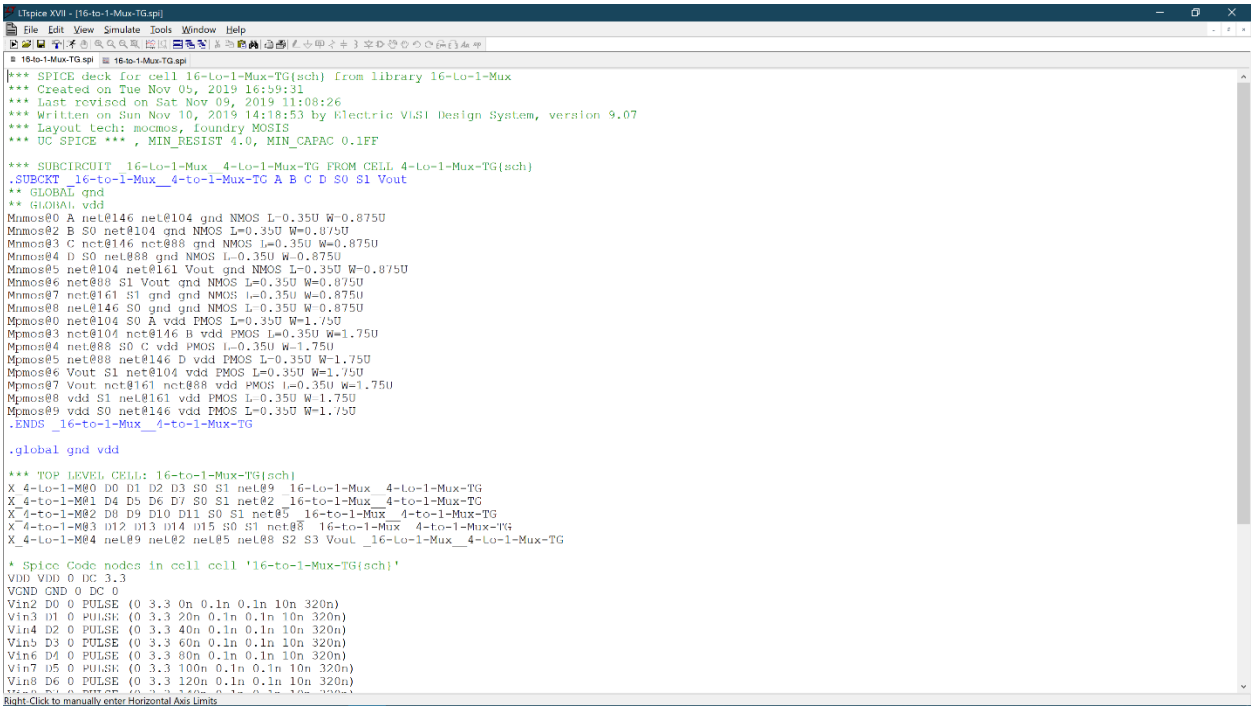

Figure 32: Generated Spice Deck of Transmission Gate 16-to-1 Multiplexer Schematic

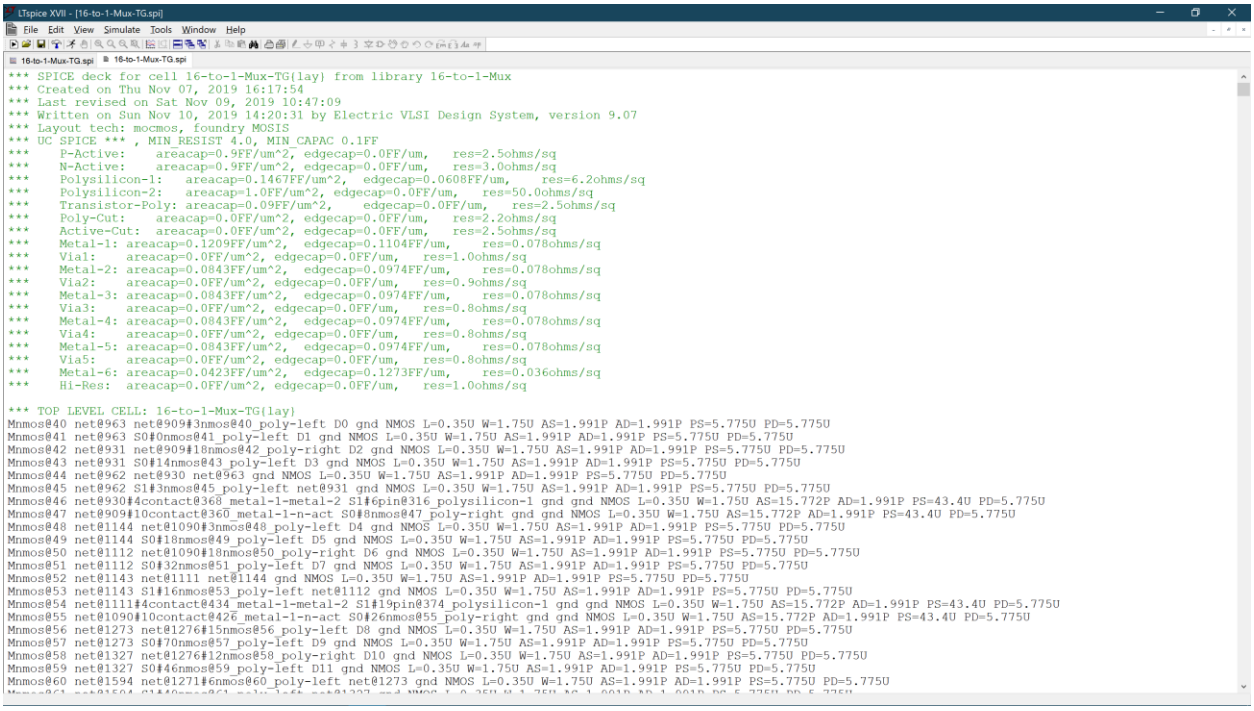

Figure 33: Generated Spice Deck of Transmission Gate 16-to-1 Multiplexer Layout

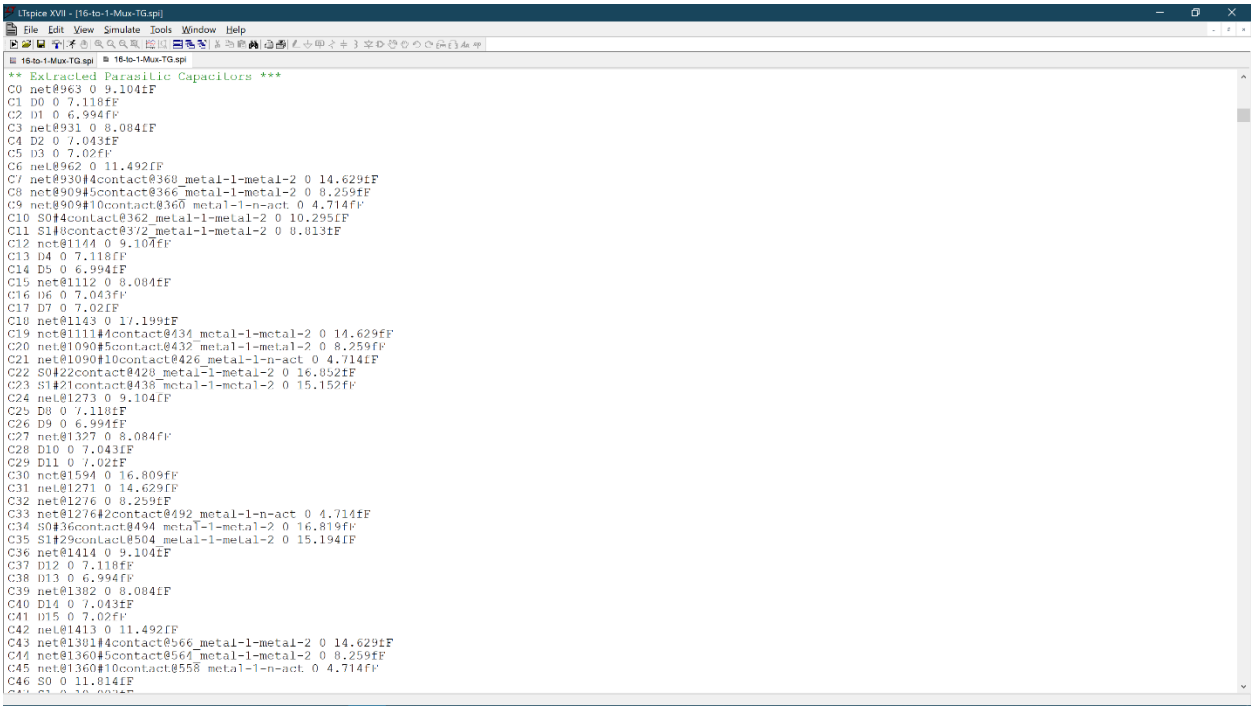

Figure 34: Extracted Parasitic Capacitors Sample of Transmission Gate 16-to-1 Multiplexer Layout

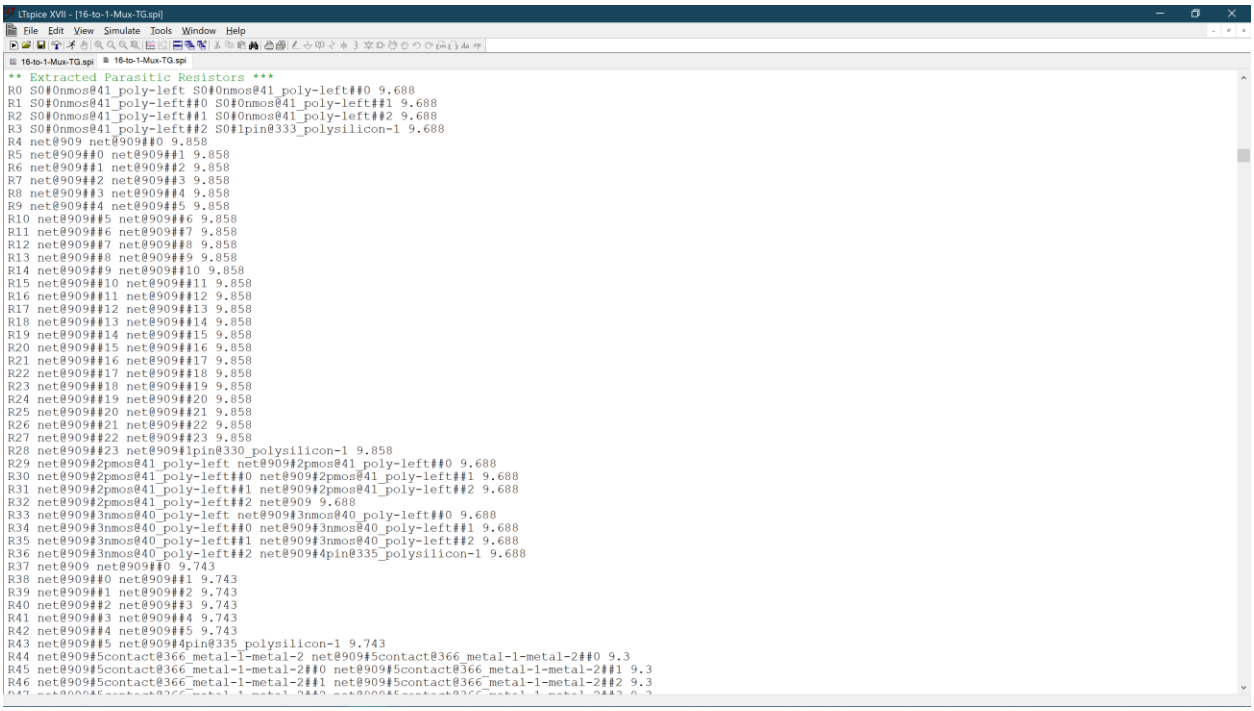

Figure 35: Extracted Parasitic Resistors Sample of Transmission Gate 16-to-1 Multiplexer Layout

Section 7: LTSPICE Simulations:

After creating the schematic and layout design of the 16-to-1 Multiplexer, waveforms were created using LTSPICE. Theses waveforms were created by using Spice Code (Figure 27) to initialize our VDD, GND, and our many inputs, D0-D15, and S0-S3, so that it could test certain computations. The computations that we tested set each input (D0-D15) for 50 nanoseconds at different times, then back to low; in other words, 100 nanoseconds period, with rise time and fall time of 5 nanoseconds and 50% duty cycle. Each of the inputs were high at different times so they wouldn't be able to relate to each other. After that, we set tested all the computations for the selector (S0-S3), starting from 0 to 15. This way, it'll be able to output each individual input and show a wavelike output. The computations that it tested are the same between the schematic and layout. We were able to verify the waveforms obtained from LTSPICE were correct by matching it with the truth table on Table 1.

Section 7.1: Schematic:

For the schematic, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the inputs and confirming that the output shows a wavelike form.

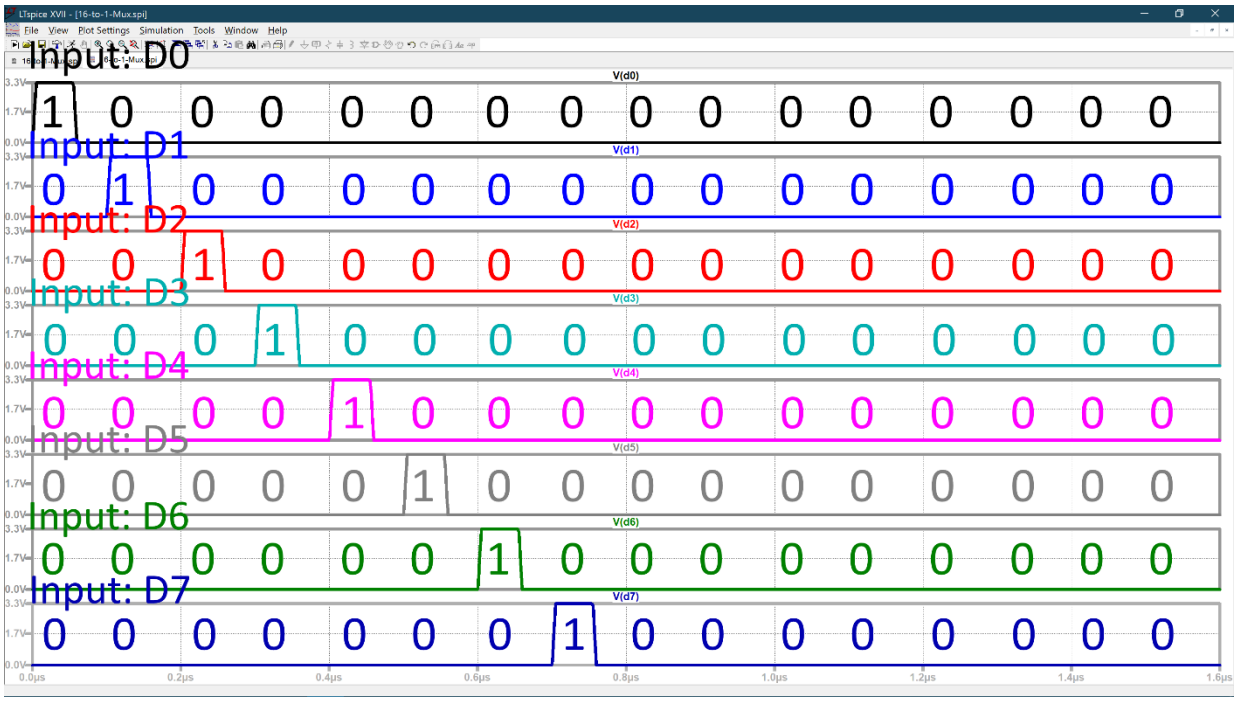

Figure 36.1: LTSPICE Waveforms of Schematic Design of a 16-to-1 Multiplexer (Inputs)

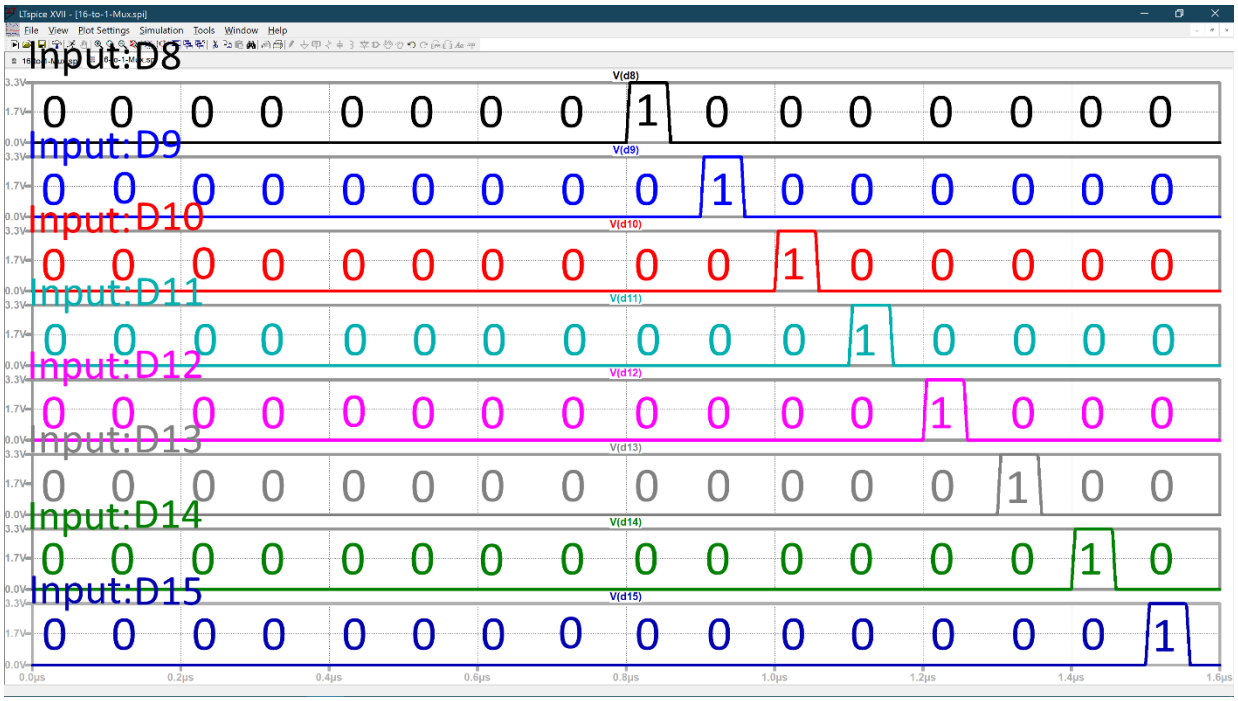

Figure 36.2: LTSPICE Waveforms of Schematic Design of a 16-to-1 Multiplexer (Inputs)

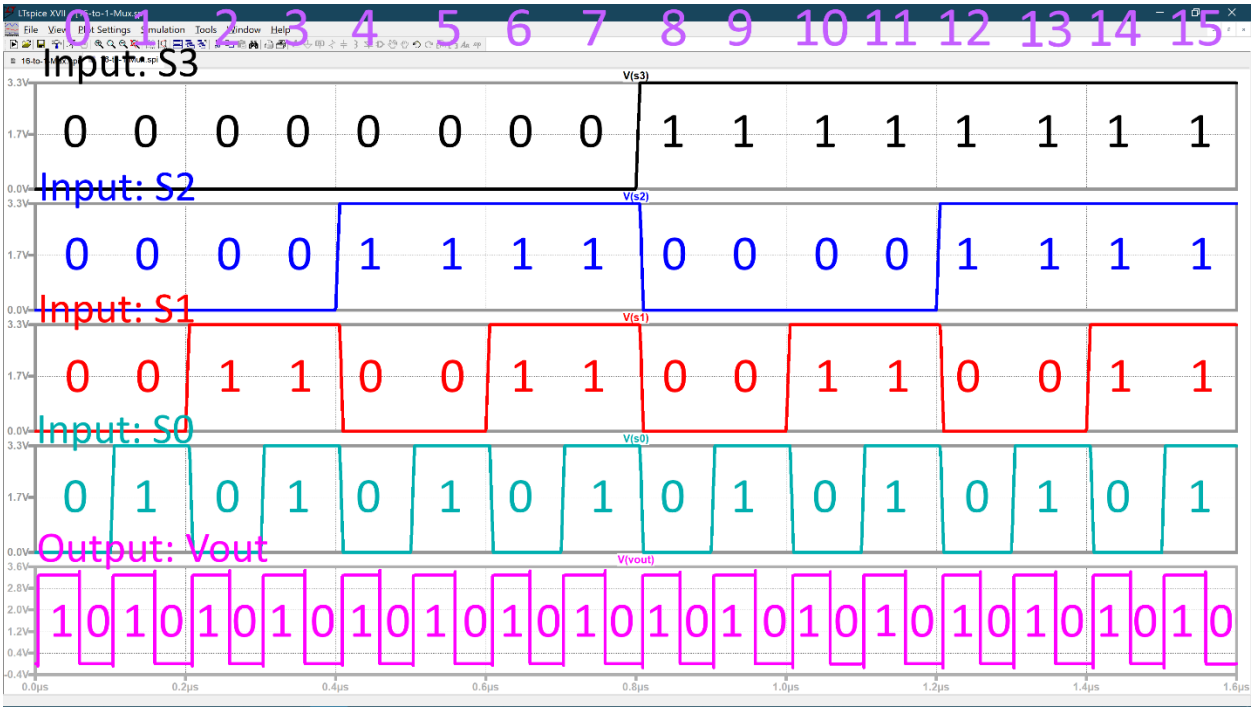

Figure 37: LTSPICE Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Outputs)

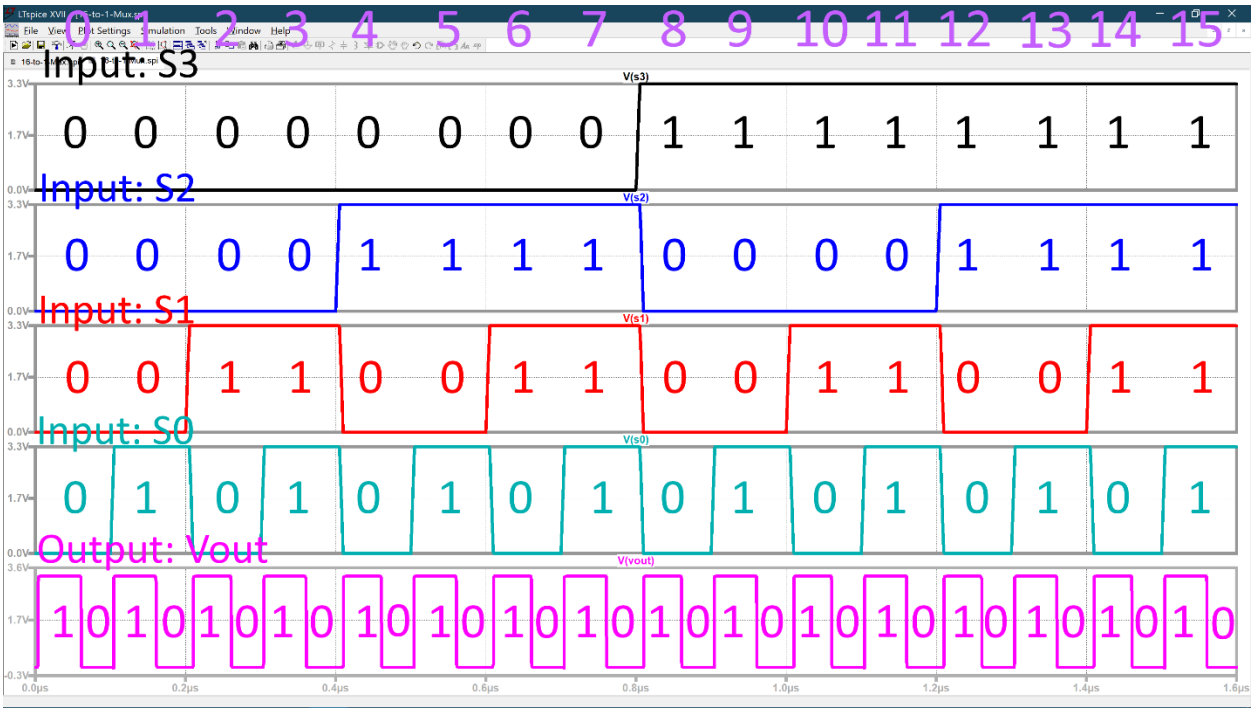

Figure 38: LTSPICE Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Outputs)

Section 7.2: Layout:

For the layout, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the inputs and confirming that the output shows a wavelike form.

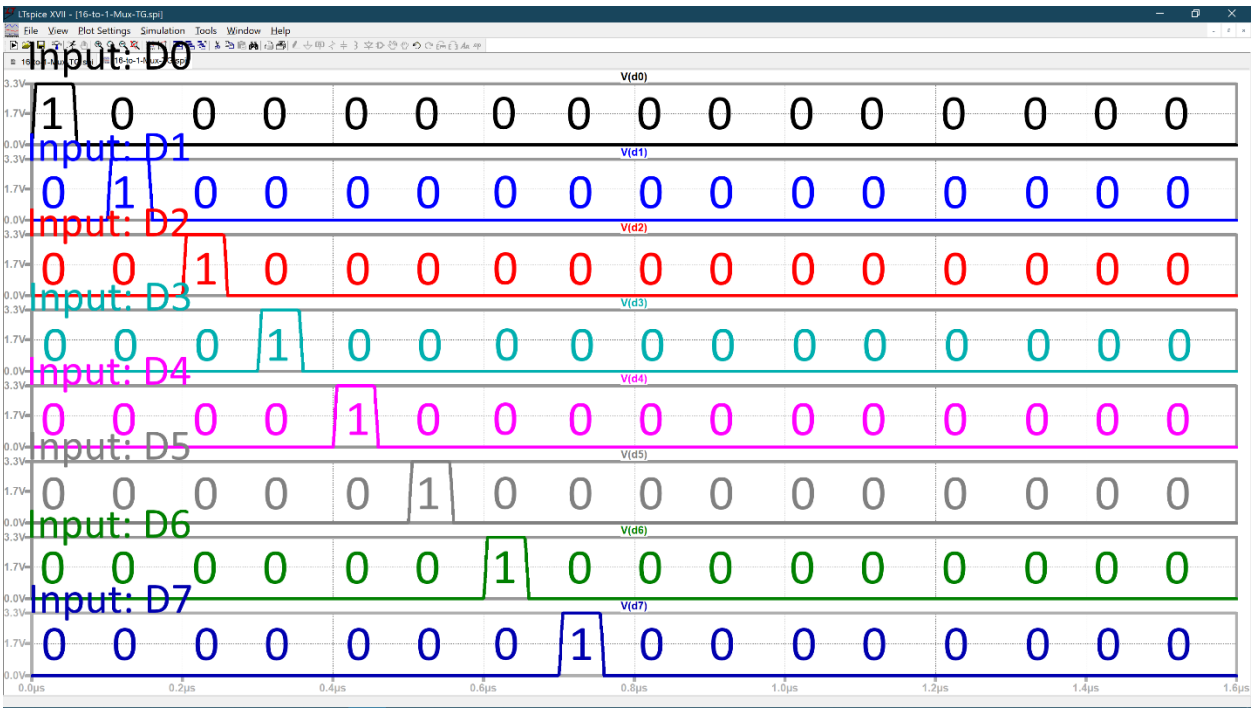

Figure 39.1: LTSPICE Waveforms of Layout Design of a 16-to-1 Multiplexer (Inputs)

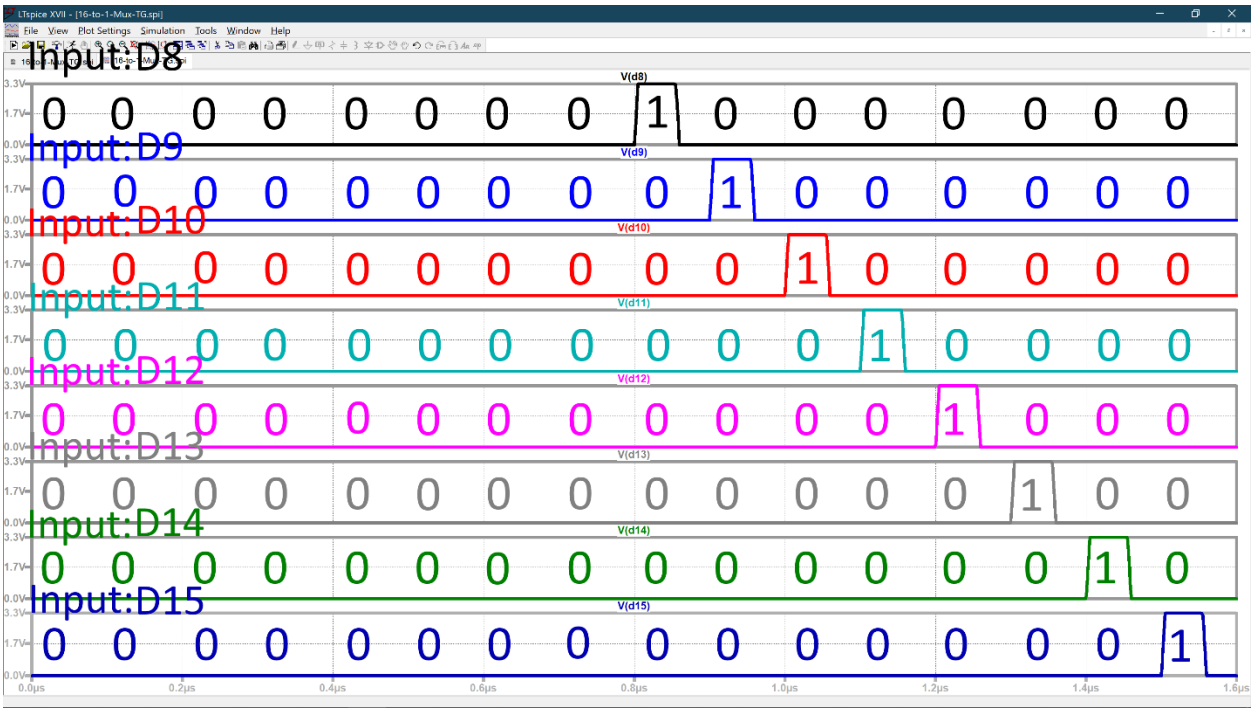

Figure 39.2: LTSPICE Waveforms of Layout Design of a 16-to-1 Multiplexer (Inputs)

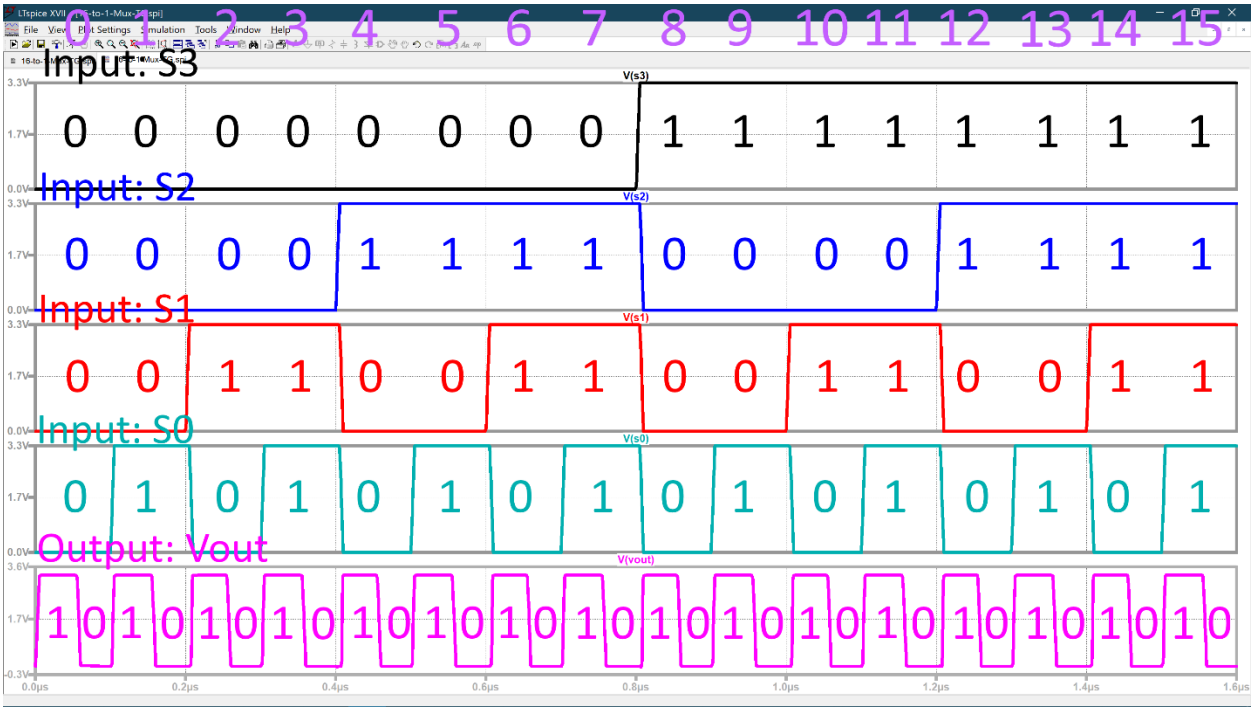

Figure 40: LTSPICE Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Outputs)

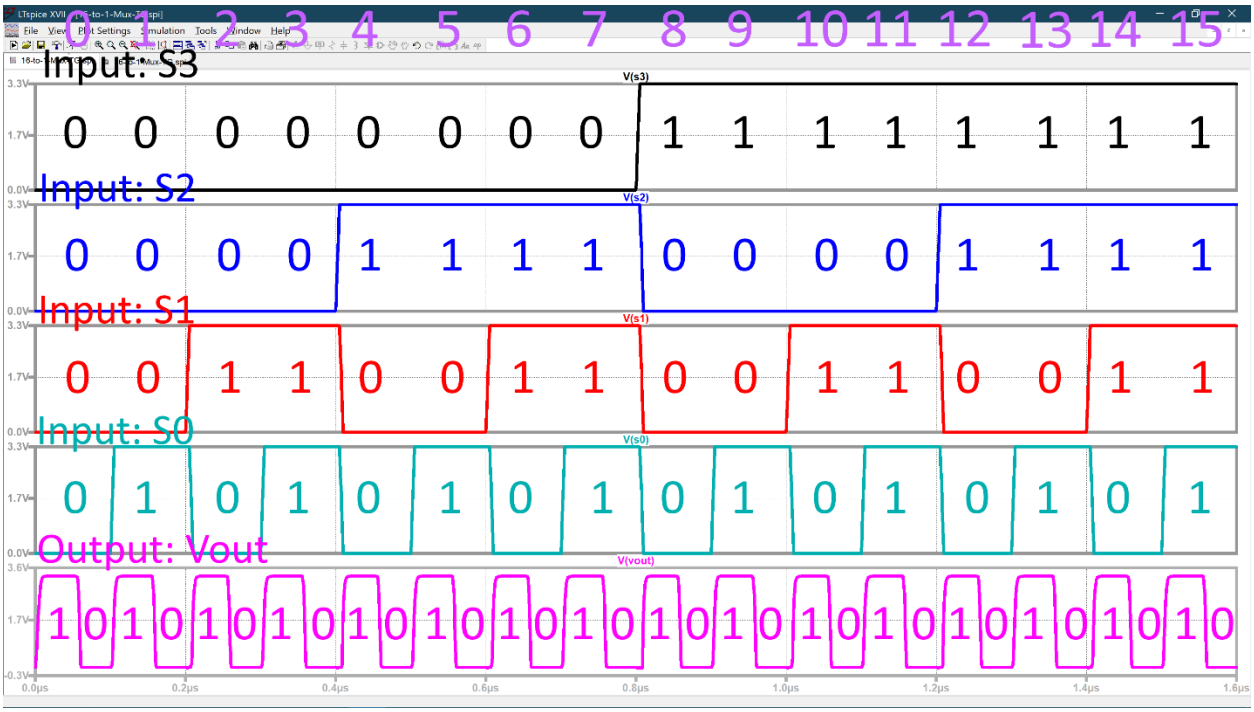

Figure 41: LTSPICE Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Outputs)

Section 7.3: Comparison:

For LTSPICE, by comparing Figure 37 (Conventional Schematic), Figure 38 (Transmission Gate Schematic), Figure 40 (Conventional Layout), and Figure 41 (Transmission Gate Layout) with each other, the way the output reacted given the certain inputs appears to be the same. In addition, with the inputs we gave, it gave us the appropriate outputs that we were looking for, so it confirms that our design is correct. The outputs that we were looking from could be seen by using the truth table on Table 1. The only noticeable difference between the figures would be the propagation delay and the way the waveforms looked, which could be seen on Table 6. For Figure 37, the output almost looks like a perfect square waveform, with similar rise and fall times; it has some parts where it peaks up. For Figure 38, the output waveform appears to have a longer fall time but appear as almost like a perfect square waveform. For Figure 40, the output waveform appears to have a longer rise time and fall time, but still appear as a square waveform (a bit curvier). For Figure 41, the output waveform appears to have a really long rise time and fall time, but still appears as a square waveform (a lot more curvier); this is probably because of the long rise time and fall time, which causes it to not stay high for very long before it has to go back to low. Depending on the which design, each has its own different propagation delay.

In conclusion, LTSPICE shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time, and propagation delay. The differences can be viewed on Table 6, which has a summary of the measurements.

Section 8: Measurement Summary:

The rise time, fall time, and propagation delay of gates of entire I/O are all shown on the table below, Table 6. It's found that for LTSPICE, the Schematic is faster compared to the Layout; the delay times are less, and it's rise and fall time are shorter. It's also found that for the IRSIM, the Schematic is faster compared to the Layout; the delay times are less. Furthermore, Table 7 provides more measurements for each of the designs, such as the transistor sizes, power dissipation, and total chip area. It's found that the transmission gate takes a lot less power and area compared to the conventional CMOS. This is because it uses less transistors compared to the conventional resulting in less power to power the transistors.

Table 6: Summary of Measurements

	Rise Time	Fall Time	Propagation Delay
Conventional LTSPICE Schematic	103.54 ns - 103.42 ns = 0.12 ns	158.92 ns - 158.72 ns = 0.20 ns	T_{HL} = 1 ns, T_{LH} = 0.90 ns
Conventional LTSPICE Layout	104.70 ns - 104.20 ns= 0.50 ns	161.37 ns - 160.65 ns = 0.72 ns	T_{HL} = 1.4 ns T_{LH} = 1.5 ns
Conventional IRSIM Schematic	N/A	N/A	Between 0.70ns - 1.55 ns
Conventional IRSIM Layout	N/A	N/A	Between 0.85 ns- 1.60 ns
Transmission Gate LTSPICE Schematic	105.20 ns - 101.20 ns = 4.00 ns	160.00 ns - 150.00 ns = 1.00 ns	T_{HL} = 0.18 ns T_{LH} = 0.20 ns
Transmission Gate LTSPICE Layout	110.00 ns - 101.00 ns = 9.00 ns	160.90 ns - 155.20 ns = 5.70 ns	T_{HL} = 0.82 ns T_{LH} = 0.85 ns
Transmission Gate IRSIM Schematic	N/A	N/A	Between 0.50 ns - 1.20 ns
Transmission Gate IRSIM Layout	N/A	N/A	Between 0.70 ns- 1.45 ns

Table 7: More Measurements

	Conventional Schematic	Conventional Layout	Transmission Gate Schematic	Transmission Gate Layout
Transistor Sizes (W/L)	PMOS (10/2), NMOS (5/2)	PMOS (10/2), NMOS (10/2)	PMOS (10/2), NMOS (5/2)	PMOS (10/2), NMOS (10/2)
Transistor Counts	Inverter = 2 AND = 6 3-AND = 6 + 6 = 12 OR = 6 4-OR = 6 + 6 + 6 = 18 4-to-1 = (4*12) + 18 + (2*2) = 70 16-to-1 = (70*5) = 350 Total = 350	3-AND = 8 4-OR = 10 Inverter = 2 4-to-1 = (8*4) + 10 + (2*2) = 46 16-to-1 = (46*5) = 230 Total = 230	4-to-1 = 16 16-to-1 = (16*5) = 80 Total = 80	4-to-1 = 16 16-to-1 = (16*5) = 80 Total = 80
Total Chip Area	X	17126.1891 um^2	X	12288.4727 um^2
Power Dissipation	3.3 V * 0.0032 A = 0.01056 Watts	3.3 V * 0.0044 A = 0.01452 Watts	3.3 V * 0.0023 A = 0.00759 Watts	3.3 V * 0.0029 A = 0.00957 Watts

Calculations:

Conventional: Size $= 1077.5\ \lambda$ x $519\ \lambda = 188562.5$ nm x $90825\ nm = 17126.1891\ \mu m^2$

Transmission Gate: Size $= 387.5\ \lambda$ x $1035.5\ \lambda = 67812.5$ nm x 181212.5 nm $=$ $12288.4727\ \mu m^2$

Section 9: Conclusion:

In this project, we designed a CMOS of a 16-to-1 Multiplexer by connecting five 4-to-1 Multiplexers together. A conventional 4-to-1 Multiplexer is designed by connecting 4 three input AND gates, 1 four input OR gate, and two inverters together. A transmission gate 4-to-1 Multiplexer is designed by connecting six transmission gates, and two inverters together. By using the Electric software, we created four different designs, a conventional schematic design, a conventional layout design, a transmission gate (TG) schematic design, and a transmission gate (TG) layout design. We also generated waveforms using two different software, IRSIM and LTSPICE. The two different software helped support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the four different design, we compared them and observe their similarities and differences. We observed that for LTSPICE and IRSIM, the input and output reacted the same way given certain inputs for both the Electric Schematic and for the Electric Layout; in addition, it matched the computed values and the goal we were trying to achieve. The only difference between the Electric Schematic and the Electric Layout were the rise time, fall time, and propagation delay. For LTSPICE and IRSIM, these forms of differences can be observed by checking out Table 6, Summary of Measurements. Another thing that we compared were the differences between conventional CMOS and transmission gates. Based off Table 7, it's found that transmission gates take less area and power compared to the conventional CMOS. This is because transmission gates are used to help simplify circuitry and because there's less transistors, there's less power needed to run all those transistors. Therefore, based on our observation and the data that was gathered, we can conclude that there isn't a significant difference in terms of the waveforms; however, there is a difference in the rise time, fall time and propagation delay when zooming in on the waveform. In addition, using transmission gates are more efficient compared to using regular convention CMOS because it saves on the amount of transistors, space, and power.

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