

EE457: Digital IC Design Fall Semester 2019 Project 3 Report Cover Sheet

Due 11/13/2019

PROJECT TITLE: <u>16-to-1 Multiplexer (MUX) Using Both Conventional CMOS and</u> <u>Transmission Gates</u>

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Put Check for completion	Topics	GRAI	DES
\checkmark	Section 1: Executive Summary		/5
\checkmark	Section 2: Introduction and Background		/5
\checkmark	Section 3: Electric Circuit Schematics		/10
\checkmark	Section 4: Detailed Electric Layouts		/25
✓	Section 5: IRSIM Logic Simulations and Measurements for Layout and Schematic (must provide comparisons between the two)		/10
✓	Section 6: LTSPICE code and <u>parasitic extractions</u> with calculation analysis for charge sharing. Put only samples of code.		/15
✓	Section 7: Measurements in LTSPICE for delays for Layout and Schematic (must provide comparisons between the two)		/15
✓	Section 8: Measurements of power, delay, chip area, timing, number of transistors for the layout.	Power Delay Area #tran	/2 /2 /2 /4
\checkmark	Section 9: Conclusion and References		/5
	Penalty		
	TOTAL	/	100

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Section 1: Executive Summary:

In this project, we will be designing a CMOS of a 16-to-1 Multiplexer (MUX) using Electric. By using the Electric software, we'll be creating four different designs, a conventional schematic design, a conventional layout design, a transmission gate (TG) schematic design, and a transmission gate (TG) layout design. The purpose for the use of the transmission gate design is for efficiency and to save on transistors. In order to test if our designs are correct, we'll be generating waveforms to test for correctness by giving a specific input and expecting a certain output. We'll be generating the waveforms using two different software, IRSIM and LTSPICE. The two different software would help support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we'll compare them and observe their similarities and differences.

To design a conventional 16-to-1 Multiplexer (MUX), we plan to use three different designs and combining them together to make a 4-to-1 Multiplexer. One design we plan to use is a three input AND gate, the second design we plan to use is a four input OR gate, and the third design we plan to use is an inverter. By combining four AND gates, one OR gates, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexers and link them together to create a 16-to-1 Multiplexer. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

To design a Transmission Gate (TG) 16-to-1 Multiplexer (MUX), we plan to use two designs and combining them together to make a 4-to-1 Multiplexer. One design we plan to use is an inverter, and the second design we plan to use is a transmission gate. By combining two inverters, and six transmission gates, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexers and link them together to create a 16-to-1 Multiplexer. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected.

Section 2: Introduction and Background:

A 16-to-1 Multiplexer is a form of digital circuit that is used to select a certain data. The 16-to-1 Multiplexer would have a total of 20 inputs and one output. 16 of the inputs are data, and the other 4 are what's used to select those data. The output would be the one of the 16 inputs, depending on what the selector selects. Multiplexers itself are often used in larger circuitry and helps a lot in terms of which data are being selected so it could be used for modification without modifying the other data. The truth table of the 16-to-1 Multiplexer is shown on Table 1.

The approach we plan to take to design the conventional 16-to-1 Multiplexer would be to use three different designs and combining them together. The three designs that we plan to use would be a three input AND gate, a four input OR gate, and an inverter. The reason for this approach is because we can't directly build a conventional 16-to-1 Multiplexer without first building a 4-to-1 Multiplexer or any Multiplexer, and we can't build a Multiplexer without using an AND gate, OR gate, or an inverter. By applying four AND gates, one OR gate, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexer and link them together to create a 16-to-1 Multiplexer. The figures on the next few pages show the schematic and layout of the two input OR gate, an inverter, and a 4-to-1 Multiplexer. In addition, the truth table of a three input AND gate is shown on Table 2; the truth table of a four input OR gate is shown on Table 3; the truth table of an inverter is shown on Table 4; the truth table of a 4-to-1 Multiplexer is shown on Table 5.

The approach we plan to take to design the transmission gate 16-to-1 Multiplexer would be to use two different designs and combining them together. The two designs that we plan to use would be a transmission gate, and an inverter. The reason for this approach is because we can't directly build a transmission gate 16-to-1 Multiplexer without first building a 4-to-1 Multiplexer or any Multiplexer, and we can't build a Multiplexer without using a transmission gate, or an inverter. By applying six transmission gates, and two inverters, we'll be able to obtain a 4-to-1 Multiplexer. After making the 4-to-1 Multiplexer, we create 4 more 4-to-1 Multiplexer and link them together to create a 16-to-1 Multiplexer. The figures on the next few pages show the schematic and layout of the 4-to-1 Multiplexer, which consists of six transmission gates, and two inverters. The truth table of a 4-to-1 Multiplexer is already shown on Table 5.

Input: S3	Input: S2	Input: S1	Input: S0	Output: 16-to-1 Multiplexer
0	0	0	0	D0
0	0	0	1	D1
0	0	1	0	D2
0	0	1	1	D3
0	1	0	0	D4
0	1	0	1	D5
0	1	1	0	D6
0	1	1	1	D7
1	0	0	0	D8
1	0	0	1	D9
1	0	1	0	D10
1	0	1	1	D11
1	1	0	0	D12
1	1	0	1	D13
1	1	1	0	D14
1	1	1	1	D15

Boolean Expression:

 $\begin{aligned} Vout &= \overline{S_0S_1S_2S_3}D_0 + S_0\overline{S_1S_2S_3}D_1 + \overline{S_0}S_1\overline{S_2S_3}D_2 + S_0S_1\overline{S_2S_3}D_3 + \\ \overline{S_0S_1}S_2\overline{S_3}D_4 + S_0\overline{S_1}S_2\overline{S_3}D_5 + \overline{S_0}S_1S_2\overline{S_3}D_6 + S_0S_1S_2\overline{S_3}D_7 + \\ \overline{S_0S_1S_2}S_3D_8 + S_0\overline{S_1S_2}S_3D_9 + \overline{S_0}S_1\overline{S_2}S_3D_{10} + S_0S_1\overline{S_2}S_3D_{11} + \\ \overline{S_0S_1}S_2S_3D_{12} + S_0\overline{S_1}S_2S_3D_{13} + \overline{S_0}S_1S_2S_3D_{14} + S_0S_1S_2S_3D_{15} \end{aligned}$

Input: A	Input: B	Input: C	Output: A AND B AND C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 2: Truth Table of a Three Input AND Gate

Boolean Expression: Vout = A * B * C

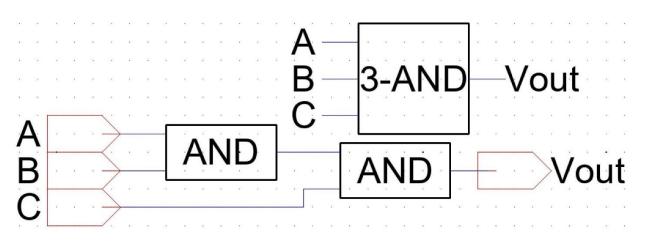


Figure 1: Schematic Design of a Three Input AND Gate

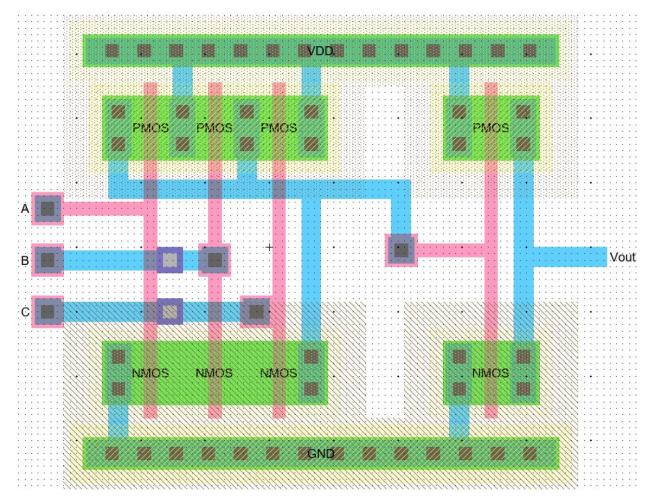


Figure 2: Layout Design of a Three Input AND Gate

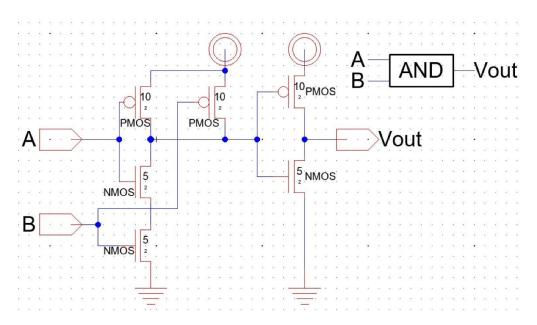


Figure 3: Schematic Design of a Two Input AND Gate That's Used

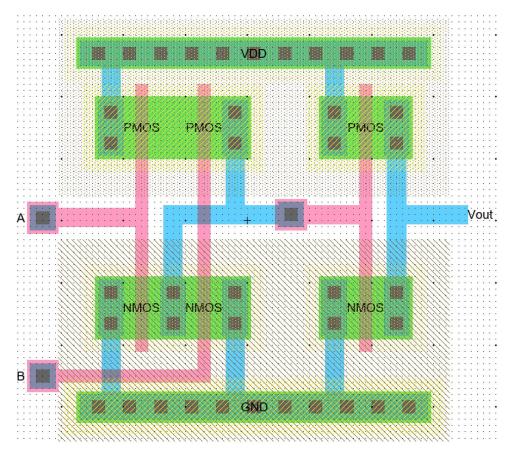


Figure 4: Layout Design of a Two Input AND Gate That's Used

Input: A	Input: B	Input: C	Input: D	Output: A OR B OR C OR D
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 3: Truth Table of a Four Input OR Gate
--

Boolean Expression: Vout = A + B + C + D

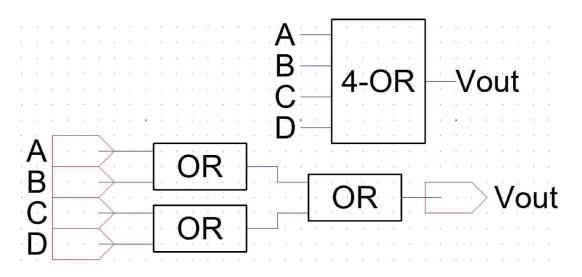


Figure 5: Schematic Design of a Four Input OR Gate

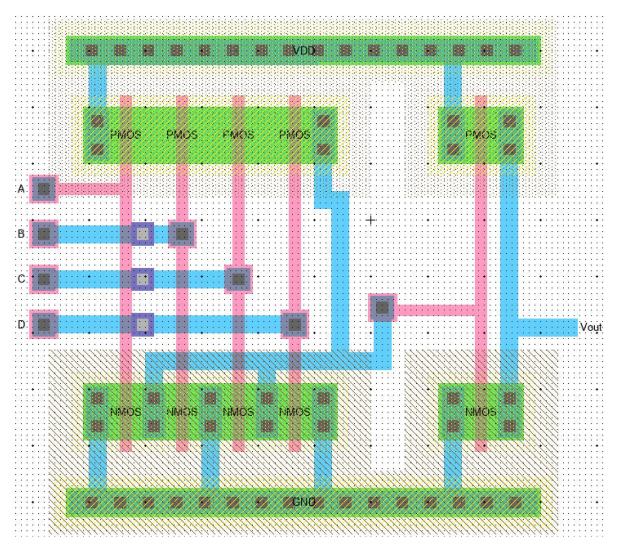


Figure 6: Layout Design of a Four Input OR Gate

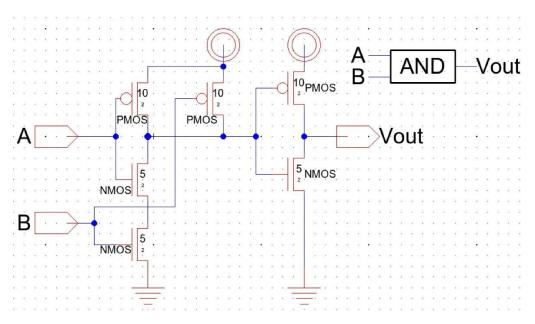


Figure 7: Schematic Design of a Two Input OR Gate That's Used

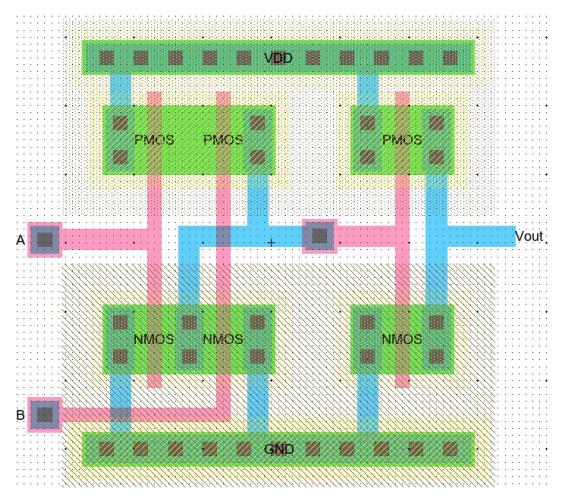
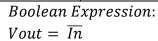


Figure 8: Layout Design of a Two Input AND Gate That's Used

1
1
0

Table 4: Truth Table of an Inverter



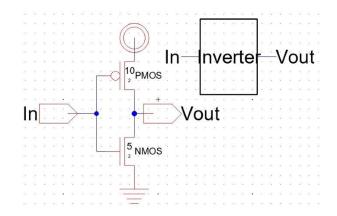


Figure 9: Schematic Design of an Inverter

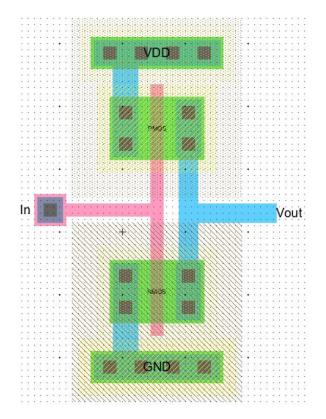
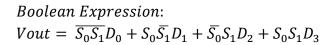


Figure 10: Layout Design of an Inverter

Input: S1	Input: S0	Output: 4-to-1 Multiplexer
0	0	A
0	1	В
1	0	С
1	1	D

Table 5: Truth Table of a 4-to-1 Multiplexer



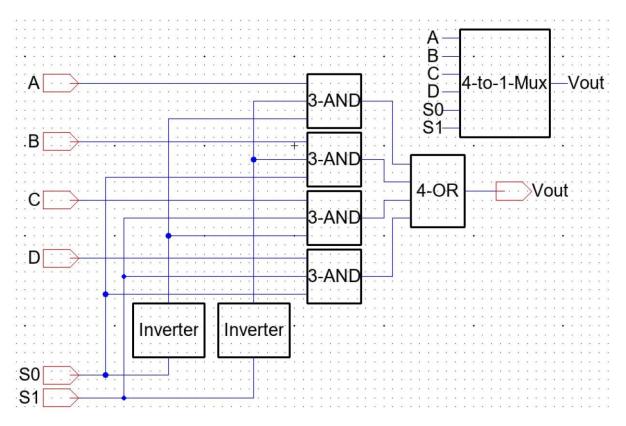


Figure 11: Schematic Design of a 4-to-1 Multiplexer

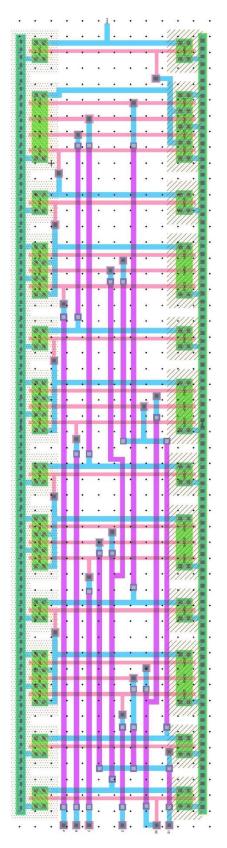


Figure 12.0: Layout Design of a 4-to-1 Multiplexer (Landscape)

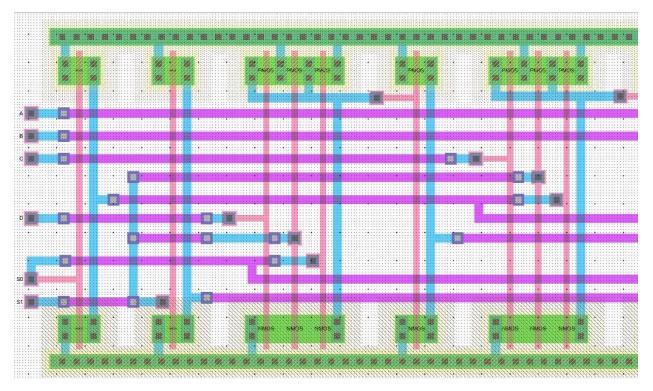


Figure 12.1: Layout Design of a 4-to-1 Multiplexer Zoomed (Left)

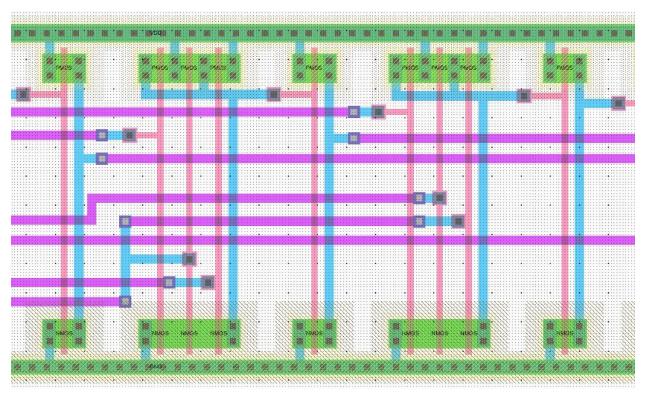


Figure 12.2: Layout Design of a 4-to-1 Multiplexer Zoomed (Middle)

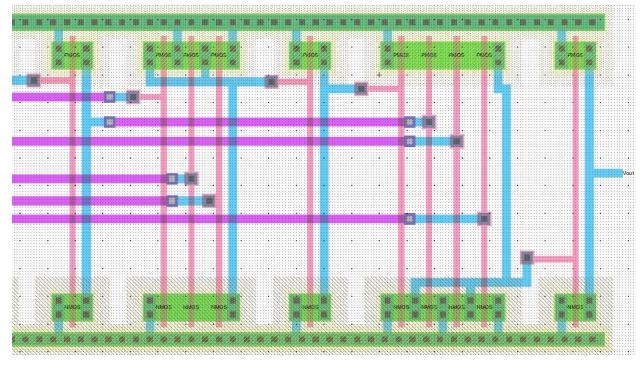


Figure 12.3: Layout Design of a 4-to-1 Multiplexer Zoomed (Right)

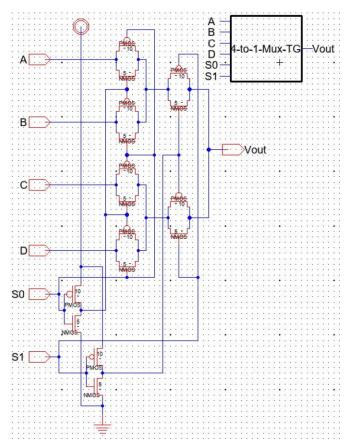


Figure 13: Schematic Design of a 4-to-1 Multiplexer Transmission Gate

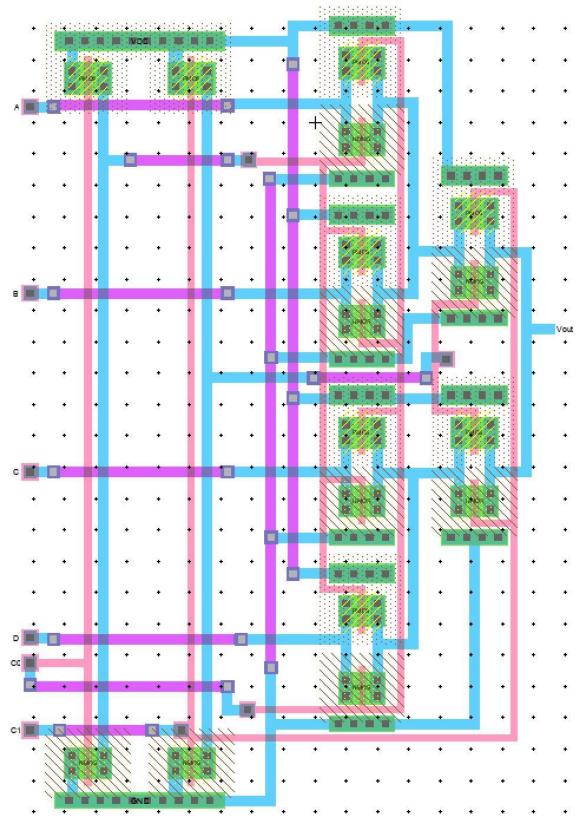


Figure 14.0: Layout Design of a 4-to-1 Multiplexer Transmission Gate

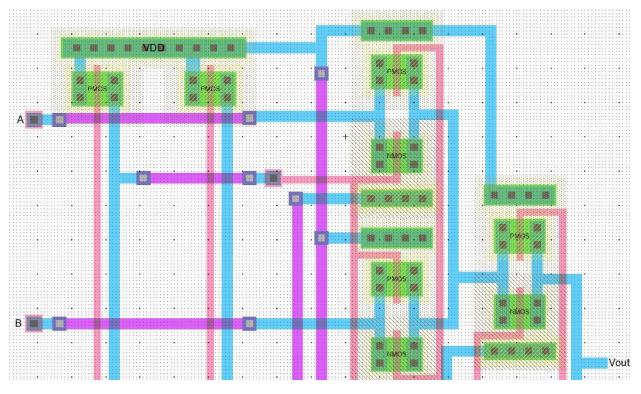


Figure 14.1: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Top)

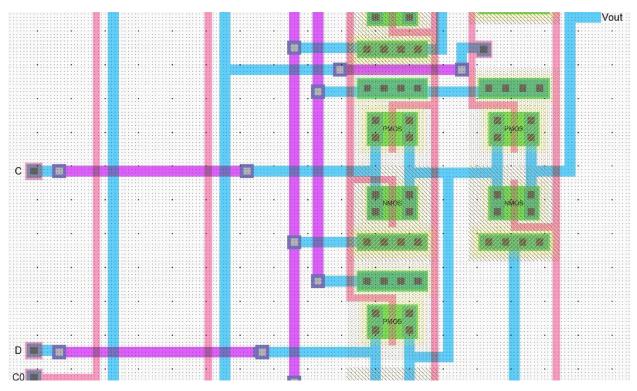


Figure 14.2: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Middle)

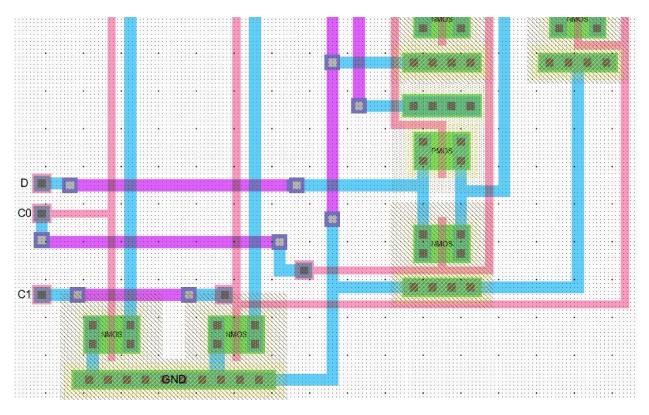


Figure 14.3: Layout Design of a 4-to-1 Multiplexer Transmission Gate Zoomed (Bottom)

Section 3: Electric Schematic:

We created a schematic of the conventional 16-to-1 Multiplexer by combining five 4-to-1 Multiplexers (Figure 11) together, using its icon. If there were any problems with the 4-to-1 Multiplexer, then we would have to go back to see the parts it was built from. In this case, the parts that it was built from are a two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, and an inverter. It was combined by connecting the output of four 4-to-1 Multiplexer to the four inputs on another 4-to-1 Multiplexer. Figure 15 shows the schematic design that was built using Electric of the conventional 16-to-1 Multiplexer. Figure 16 shows the Design Rule Check (DRC) that was performed on the schematic for the conventional 16-to-1 Multiplexer; it indicates that there were no errors or warning with the schematic.

For the transmission gate 16-to-1 Multiplexer, it's created by combining five transmission gate 4-to-1 Multiplexer (Figure 13). It was combined by connecting the output of four transmission gate 4-to-1 Multiplexer to the four inputs on another transmission gate 4-to-1 Multiplexer. Figure 17 shows the schematic design that was built using Electric of the transmission gate 16-to-1 Multiplexer. Figure 18 shows the Design Rule Check (DRC) that was performed on the schematic for the transmission gate 16-to-1 Multiplexer; it indicates that there were no errors or warning with the schematic.

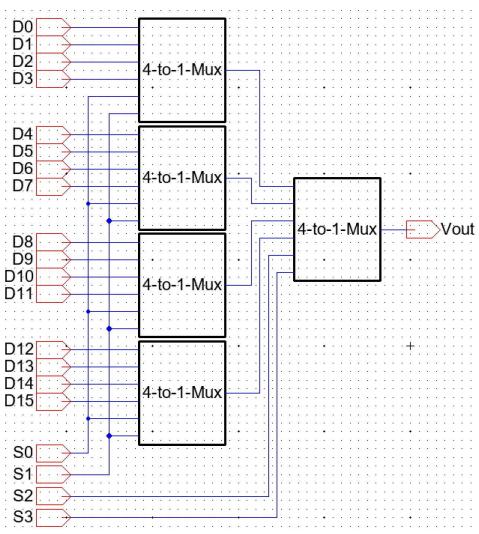


Figure 15: Schematic Design of a 16-to-1 Multiplexer

😟 Electric Messages	
55	
Checking schematic cell 'AND{sch}'	
No errors found	
Checking schematic cell '3-AND{sch}'	
No errors found	
Checking schematic cell 'OR{sch}'	
No errors found	
Checking schematic cell '4-OR{sch}'	
No errors found	
Checking schematic cell 'Inverter{sch}'	
No errors found	
Checking schematic cell '4-to-1-Mux{sch}'	
No errors found	
Checking schematic cell '16-to-1-Mux{sch}'	
No errors found	
0 errors and 0 warnings found (took 0.031 secs)	

Figure 16: Design Rule Check (DRC) of a 16-to-1 Multiplexer Schematic Design

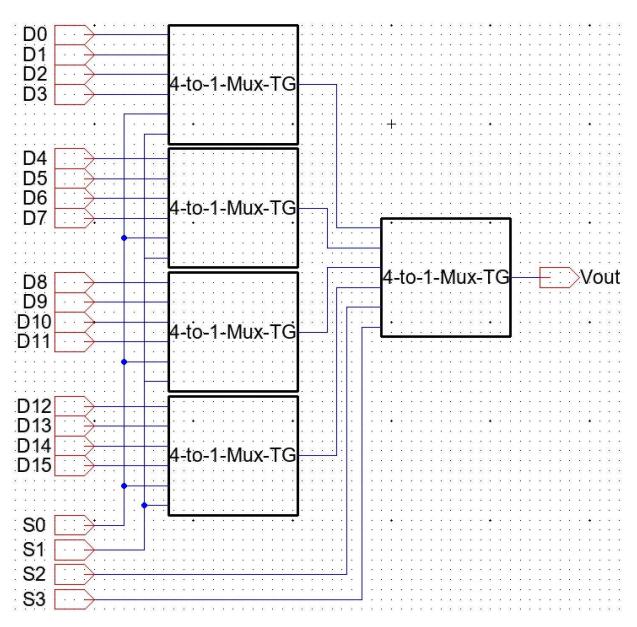


Figure 17: Schematic Design of a 16-to-1 Multiplexer Transmission Gate

Electric Messages	======9================================
Checking schematic cell	'4-to-1-Mux-TG{sch}'
No errors found	
Checking schematic cell	'16-to-1-Mux-TG{sch}'
No errors found	
0 errors and 0 warnings	found (took 0.031 secs)

Figure 18: Design Rule Check (DRC) of a 16-to-1 Multiplexer Transmission Gate Schematic Design

Section 4: Electric Layout:

We created a layout of the conventional 16-to-1 Multiplexer by combining five 4-to-1 Multiplexers (Figure 12) together. If there were any problems with the 4-to-1 Multiplexer, then we would have to go back to see the parts it was built from. In this case, the parts that it was built from are a two input AND gate, which becomes a three input AND gate, two input OR gate, which becomes a four input OR gate, and an inverter. It was combined by connecting the output of four 4-to-1 Multiplexer to the four inputs on another 4-to-1 Multiplexer. Figure 19 shows the layout design that was built using Electric of the conventional 16-to-1 Multiplexer. There is an overview and a zoomed version of the layout since the overview isn't clear enough. In addition, if additional justifications are needed, refer to Figure 12. Figure 20 shows the Design Rule Check (DRC) and Well Check that was performed on the layout for the conventional 16-to-1 Multiplexer; it indicates that there were no errors or warning with the layout.

For the transmission gate 16-to-1 Multiplexer, it's created by combining five transmission gate 4-to-1 Multiplexer (Figure 14). It was combined by connecting the output of four transmission gate 4-to-1 Multiplexer to the four inputs on another transmission gate 4-to-1 Multiplexer. Figure 21 shows the layout design that was built using Electric of the transmission gate 16-to-1 Multiplexer. There is an overview and a zoomed version of the layout since the overview isn't clear enough. In addition, if additional justifications are needed, refer to Figure 14. Figure 22 shows the Design Rule Check (DRC) and Well Check that was performed on the layout for the transmission gate 16-to-1 Multiplexer; it indicates that there were no errors or warning with the layout.

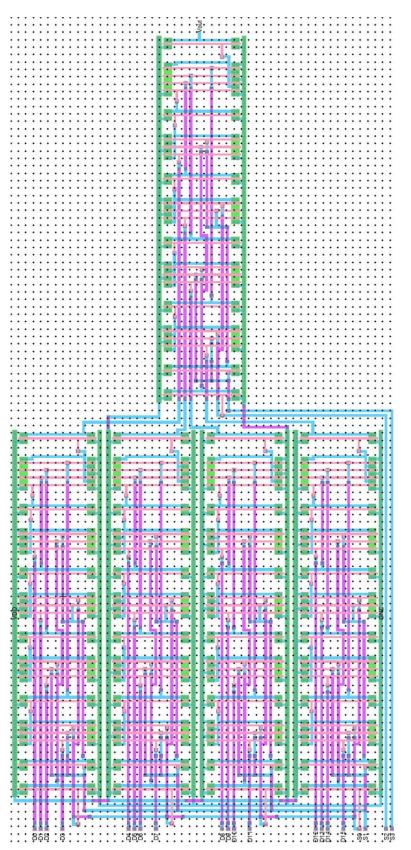


Figure 19.0: Layout Design of a 16-to-1 Multiplexer (Landscape)

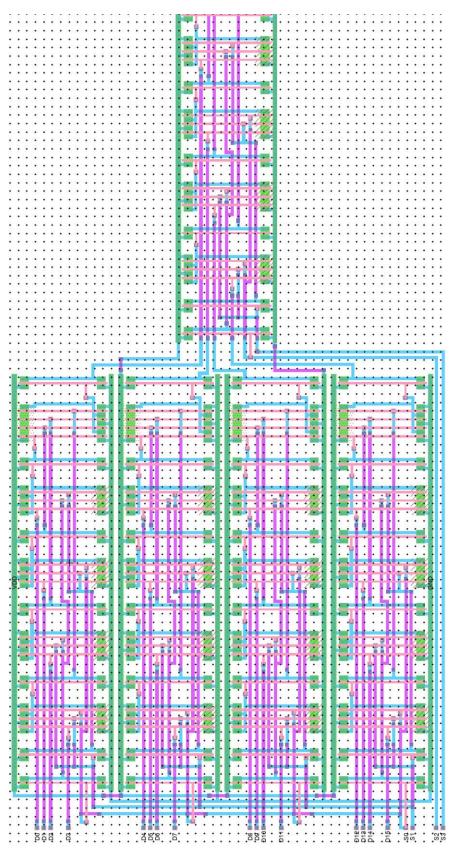


Figure 19.1: Layout Design of a 16-to-1 Multiplexer Zoomed (Landscape)

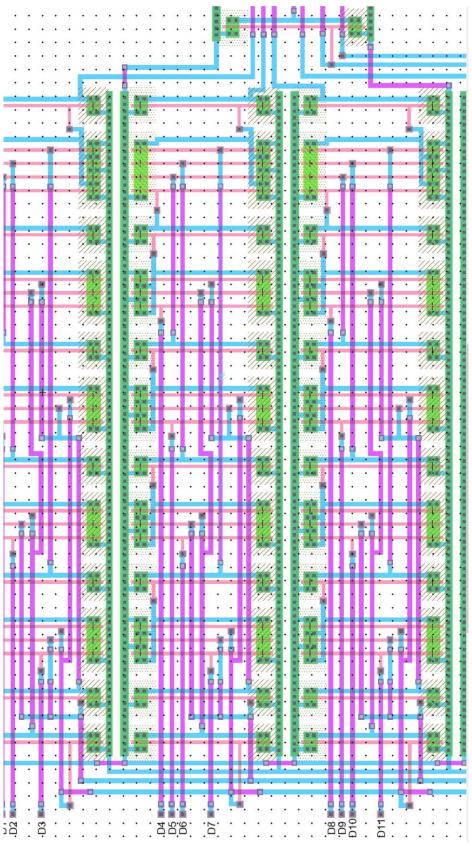


Figure 19.2: Layout Design of a 16-to-1 Multiplexer Zoomed (Landscape)

😟 Electric Messages

_____6_____6_____6_____6_____ Running DRC with area bit on, extension bit on, Mosis bit Checking again hierarchy (0.016 secs) Found 368 networks Checking cell '16-to-1-Mux{lay}' No errors/warnings found 0 errors and 0 warnings found (took 4.329 secs) ==========7=====7================ Checking Wells and Substrates in '16-to-1-Mux:16-to-1-Mux{lay}' ... Geometry collection found 940 well pieces, took 0.101 secs Geometry analysis used 4 threads and took 0.022 secs NetValues propagation took 0.0 secs Checking short circuits in 10 well contacts Additional analysis took 0.0 secs No Well errors found (took 0.123 secs) Figure 20: Design Rule Check (DRC) and Well Check of a 16-to-1 Multiplexer Layout Design

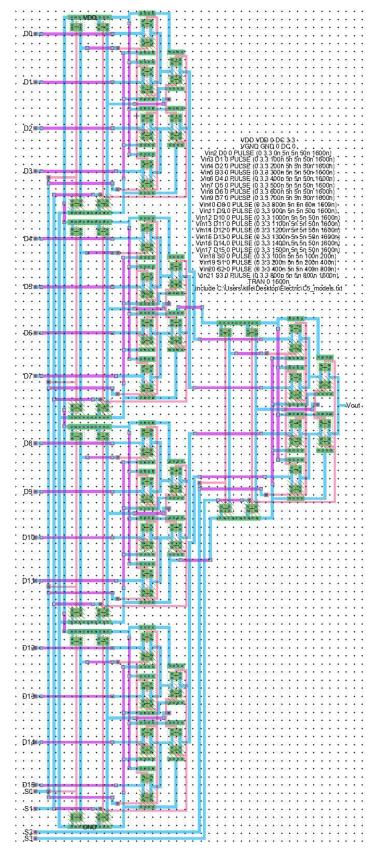


Figure 21.0: Layout Design of a Transmission Gate 16-to-1 Multiplexer

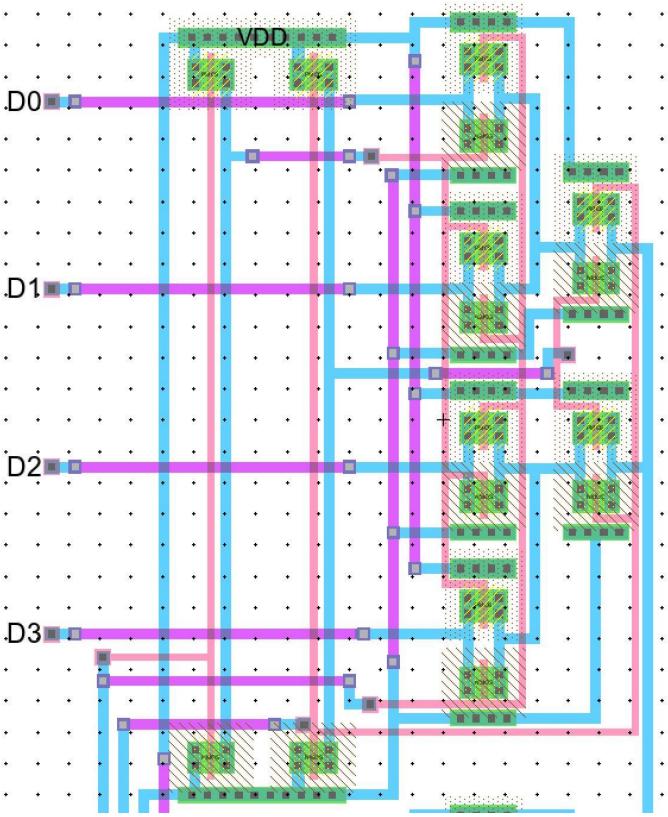


Figure 21.1: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Top)

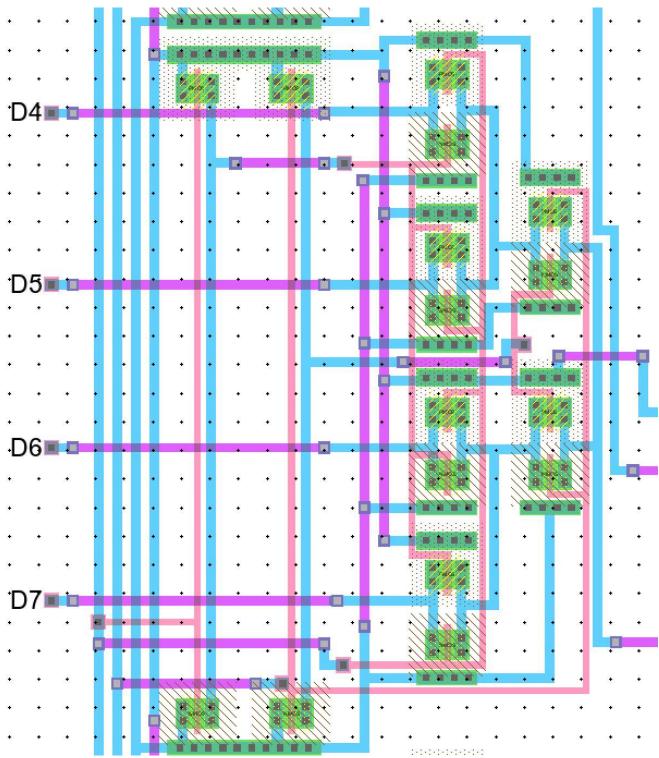
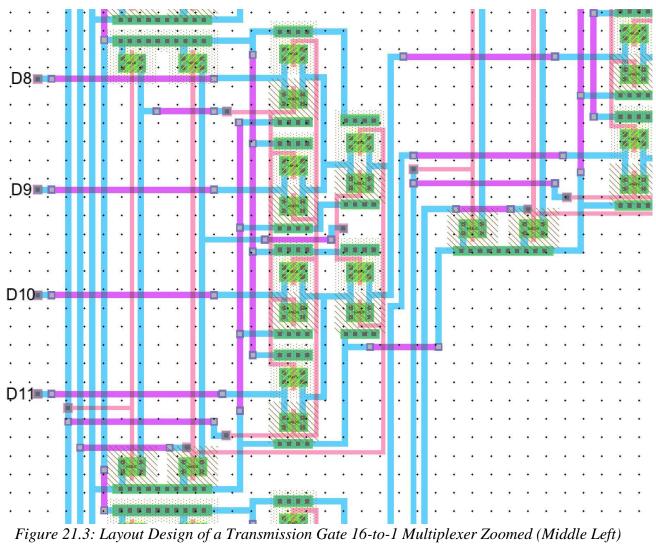
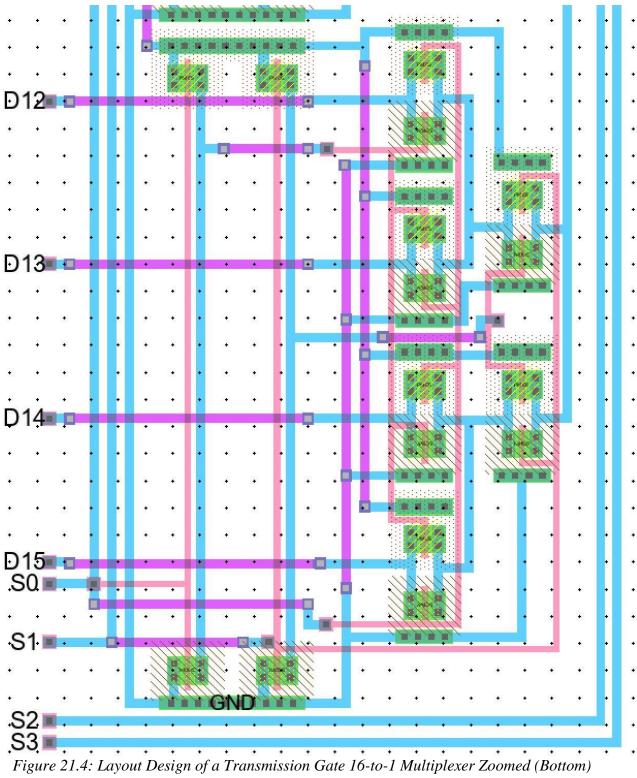
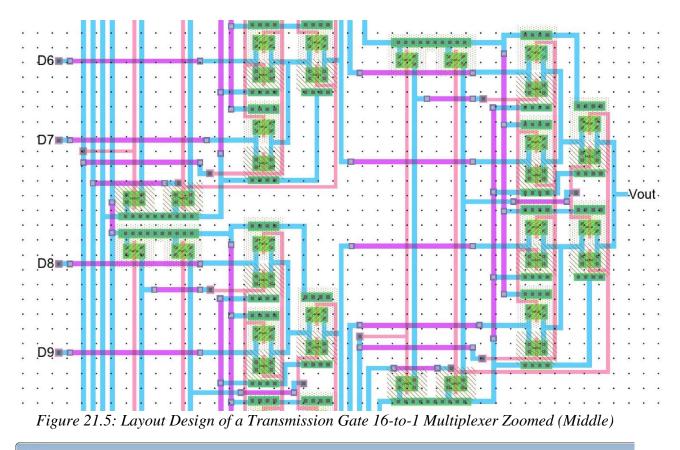


Figure 21.2: Layout Design of a Transmission Gate 16-to-1 Multiplexer Zoomed (Middle Left)







Electric Messages

Figure 22: Design Rule Check (DRC) and Well Check of a Transmission Gate 16-to-1 Multiplexer Layout Design

Section 5: IRSIM Simulations:

After creating the schematic and layout design of the 16-to-1 Multiplexer, waveforms were created using IRSIM. Theses waveforms were created by configuring the inputs, D0-D15, and S0-S3, so that it could test certain computations. The computations that it tested are the same between the schematic and layout. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify the waveforms obtained from IRSIM were correct by matching it with the truth table on Table 1.

Section 5.1: Schematic:

For the schematic, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the selectors and counting the peaks for the one that's selected and comparing it with the output.

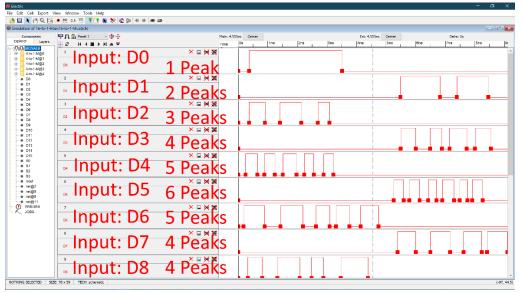


Figure 23.1: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer

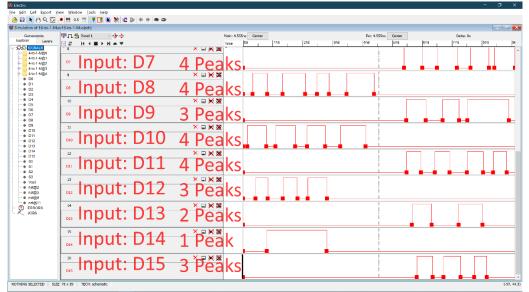


Figure 23.2: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer

😟 Electric				– 0 ×
File Edit Cell Export Vi	iew Window Tools Help • # 0.5 🗮 👎 🔁 🖹 📽 📽 🕼 + 🔿 👄		0	1
Simulation of 16-to-1-Mu	nc16-to-1-Mux{sch}		•	- 8 ×
Components Explorer Layers	罕几品 Panel 17	Main: 5.001ns Time	Center Ext: 5.001 Cis 1ns 2ns 3ns 4ns	ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns
4-to-1-M@0 4-to-1-M@1 4-to-1-M@2 4-to-1-M@3	¹⁷ Input: S3	× ⊑ ¥ ¥	0	0
	[™] Input: S2	× 🗆 💥 🔀	0	0
	¹⁹ Input: S1	×口减援	0	0
D9 D10 D11 D12 D13	[®] Input: SO	× 🗆 💥 💥	0	1
	^a Output: Vout	× • × × × × × 3 Peaks	Delay	Delay
		1 Peak		
LERRORS JOBS	^a Input: D1	2 Peaks		
NOTHING SELECTED SIZE	: 78 x 59 TECH: schematic			(-104, 46)

Figure 23.3: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 0 and 1)

😃 Electric				- 0 X			
Eile Edit Cell Export V	jew Window Iools Help 🧈 拱 0.5 👯 👎 🍞 🐚 💸 📽 😭 🐗 🗭 👄		2				
Simulation of 16-6-1-Muricho-1 Muricho-1							
Components Explorer Layers	Ლ几급 Panel 1 ∨ ग्रेंग * ﷺ ८ N	Main: 5.033ns Time	Center Ext: 5.03 Ds 1ns 2ns 3ns 4ns	3ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns 1			
4-to-1-M@0 4-to-1-M@1 4-to-1-M@2 4-to-1-M@3	¹ Input: S3	× 🗆 💥 💥	0	0			
Image: Horst-Naligital Image: Horst-Naligital <	² Input: S2	× 🗆 💥 🐹	0	0			
	³ Input: S1	× u jų jų	1	1			
	[•] Input: SO	× 🗆 💥 💥	0	1			
	Cutput: Vou	t 7 Peaks	Delay	Delay			
	[•] Input: D2	3 Peaks					
	[°] Input: D3	4 Peaks					
VOTHING SELECTED SIZE: 78 x 59 TECH: sobemaic (-99.5, 46)							

Figure 23.4: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 2 and 3)

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Simulation of 16-to-1-Mu	ux16-to-1-Mux{sch}			- 8 🗙	
Components Explorer Layers	罕 ∏ 🔠 Panel 1 → ग्रैंग 💠 ⅲ 🖉 । स र 🔳 ト म 🔺 🗢	Main: 4.894ns G Time Os	enter 1ns 2ns 3ns 4ns	Ext: 4.894ns Center Delta: 0s 5 5ns 6ns 7ns 8ns 9ns	
⇒ District Friend 4-0-144(g) Friend 6-0-144(g) Friend 0-12 - 0-12 - 0-12 - 0-12 - 0-10 - 0-11 - 0-11 - 0-11 - 0-15 - 0-15 - 0-15 - 0-15 - 0-15 - 0-16 - 0-16 - 0-16 - 0-16 - 0-16 - 0-16 - 0-16 - 0-16	[⊥] Input: S3	× □ ¥ ¥	0	0	
	² Input: S2	× □ ¥ ₩	1	1	
	³ Input: S1	× □) x () x	0	0	
	[•] Input: SO	× □	0	1	
	Output: Voi	Jt × ■ × × × × × L	Delay	Delay	
	¦¶Input: D4	5 Peaks			
	[*] Input: D5	6 Peaks			
NOTHING SELECTED SIZE: 78 x 59 TECH: sohematic (495.5, 46)					

Figure 23.5: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 4 and 5)

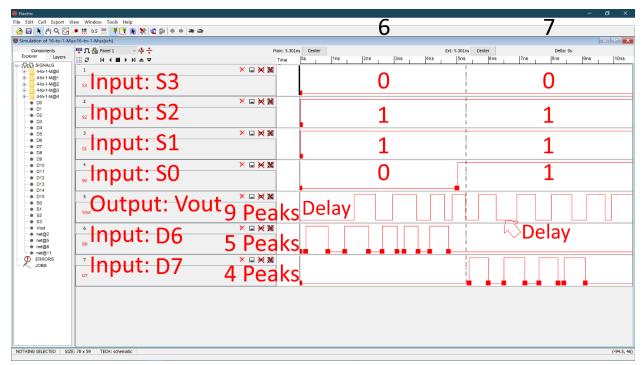


Figure 23.6: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 6 and 7)

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				- 7 🗙
Explorer Layers	₩µ∏aapanel1 ∨ŵr∳ ∰ 2 H I∎ F H ≜ マ	Time 0s	Center 1ns 2ns 3ns 4ns	Ext: S.213ns Center Delta: 0s 5na 6na 7ns 8na 9ns 10ns
4-to-1-M@0 4-to-1-M@1 4-to-1-M@2 4-to-1-M@3	¹ Input: S3	× □ ½ ¥	1	1
	² Input: S2	× □ ¥ ₩	0	0
D5 D6 D7 D8	³ Input: S1	× 🗆)ví 💥	0	0
• D7	Input: SO	× □ ¥ 鯊	0	1
D15 S0 S1 S2	Output: Vou	t 7 Peaks	Delay	
	[°] Input: D8	× □ 涎 溅		⊳Delay
	ⁱ Input: D9	3 Peaks		
NOTHING SELECTED SIZE	<pre>End Cell Expert View Window Tods Holp 8 _ 9 _ 9 _ 0 _ 0 _ 0 _ 0 _ 0 _ 0 _ 0 _ 0</pre>			

Figure 23.7: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 8 and 9)

			10	- • × 11
	• # 0.5 # • • • • • • • •		10	
Components Explorer Layers	₩₩₩₩₩₩₩₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩	Main: 5.163ns Time	Center Ds 1ns 2ns 3ns 4ns	Ext: 5.163ns Center Delta: 0s 500 500 500 500 500 500 500 500 500
4-to-1-M@0 4-to-1-M@1 4-to-1-M@2 4-to-1-M@3	[™] Input: S3	× 🗆 💥 🐹	. 1	1
File Edit Cell Export View Image: Simulation of 16-16-14.uc(3) Image: Simulation of 16-16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) Image: Simulation of 16-14.uc(3) <t< td=""><td>° Input: S2</td><td>× • ¥ ¥</td><td>0</td><td>0</td></t<>	° Input: S2	× • ¥ ¥	0	0
	input: S1	× • × ×	1	1
- • D10 - • D11 - • D12 - • D13	[•] Input: SO	× 🗆 💓 💥	0	1
	⁵ Output: Vou	t ^{× • × ×} 8 Peaks	Delay	Delay
	[•] Input: D10	4 Peaks		
	⁷ Input: D11	4 Peaks		
NOTHING SELECTED SIZE	78 x 59 TECH: schematic			(-75.5, 41)

Figure 23.8: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 10 and 11)

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-				- 🕫 🗙
Explorer Layers	♀ □ 冊 Panel 1 → ♪ ↓ ▲ マ	Main: 4.762r Time	ns Center Ext: 4.762	ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns
E ALA SIGNALS				
File Edit Cell Export View Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image: Simulation of 16-to-14/unc16 Image:	Input: S3		1	1
	^² Input: S2	*	1	1
D5 D6 D7 D8	^³ Input: S1 × ∞ ×	*	0	0
• D10 • D11 • D12 • D13	[∗] ∎×	*	0	1
	. Output: Vout ₅ Pe	* aks	Delay	Delay
S0 S1 S2 S3 Vout enet@2 enet@2 enet@3 enet@3 enet@1 enet@1 fnet@1	Input: D12 3 Pe	aks		
	[*] Input: D13 2 [*] Pe	aks		
	78 x 59 TECH: schematic			(-104, 46)
NOTING OLLECTED SIZE	170 X 22 TECH VERSING			(*107, 10)

Figure 23.9: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 12 and 13)

😲 Electric					- 🗆 X
			14		15
1			± 1		<u>_</u>
File Edit Cell Export Yiew W Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulation of 16-to-1440ct Edit Image: Simulatio Edit Image: Simula	弾れ品 Panel 1 √ ∲ ∻ … ジ ダ N イ ■ ▶ N ▲ ▼	Main: 4.819ns Time	Center Ins 2ns 3ns		
File Edit Cell Expot View V Image: State of the state of	¹ Input: S3	× u ¥ ¥	1		1
	^² Input: S2	× 🖬 💥 💥	1		1
	Input: S1	× u ¥ ¥	1		1
- • D10 - • D11 - • D12 - • D13	. Input: SO	× u x X	0		1
	^s Output: Vout	4 Peaks	Delay		Delay
	$^{\circ}$ loop to \mathbf{D}	🗙 🖬 📈 🕱			
	['] Input: D15	3 Peaks			
Image: Second and Second				(-88.5, 36)	

Figure 23.10: IRSIM Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Selector at 14 and 15)

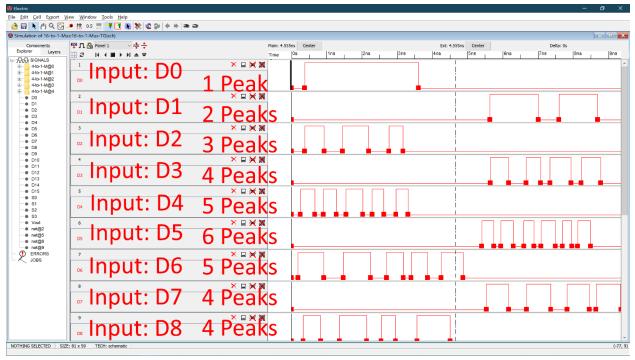


Figure 24.1: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer

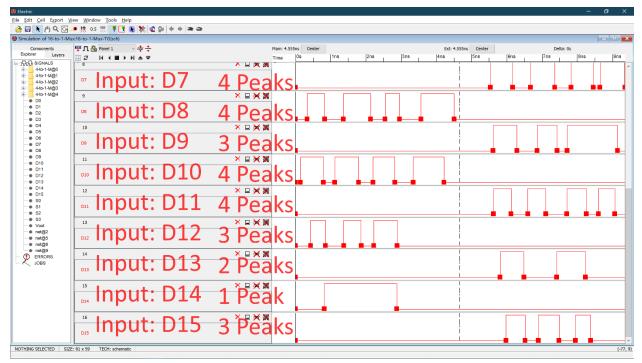


Figure 24.2: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer

🙂 Electric				– 61 ×
	ew Window Iools Help ● 拱 0.5 読 👎 👎 🔥 💸 📽 😭 🔶 👄 👄		0	1
Simulation of 16-to-1-Mux	x:16-to-1-Mux-TG(sch)		0	- # ×
Explorer Layers	Ლ几급 Panel 17 ∨ ‡ * ⅲ ८ । । । ■ ► н ▲ マ	Main: 5.001ns Time	Center Ext: 5.001 0s 1ns 2ns 3ns 4ns	ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns
Bile Edit Call Export Verv Verv Simulation Concorrents Layers Export II Export Export Layers II Image: Simulation Ado:1AMQ2 II II Image: Simulation Ado:1AMQ2 III III Image: Simulation III III IIII Image: Simulation IIII IIII IIII Image: Simulation IIII IIII IIII Image: Simulation IIIII IIII IIIII Image: Simulation IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	["] Input: S3	× • ¥	0	0
© D0 © D1 © D2 © D3	[™] Input: S2	× 🗆 💥 💥	0	0
© D5 © D6 © D7 © D8	¹⁹ Input: S1	× u x	0	0
+ D10 + D11 ++ D12 ++ D13	[®] Input: SO	× 🗆 💥 💥	0	1
D15 \$0 \$1 \$2	Cutput: Vout	× • × × × × × × × × × × × × × × × × × ×	Delay	Delay
••• Vout ••• net@2 ••• net@5 ••• net@8	["] Input: D0	1 Peak		
• net@9	^{aa} Input: D1	2 Peaks		
NOTHING SELECTED SIZE:	t : 81 x 59 TECH: schematic			(-77, 9)

Figure 24.3: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 0 and 1)

😃 Electric				– 6 ×
			2	3
			Ζ	J – 🖻 💌
Bile Edit Call Earort Yew Yew Image: State of the	Ლ几冊 Panel 1 ∨ № ☆ ## ८ N N N N A ♥	Main: 5.033ns Time 01	Center Ext: 5.033 s 1ns 2ns 3ns 4ns	ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns 1
	[•] Input: S3	× • ¥ ¥	0	0
	² Input: S2	× 🗆 💥 🐹	0	0
© D5 © D6 © D7 © D8	input: S1	× 🗆 💓 💥	1	1
+ D10 + D11 + D12 + D13	. Input: SO	× □ ¥ X	0	1
D15 S0 S1 S2	Output: Vou	t ^{× •} ** 7 Peaks	Delay	Delay
	¹ Input: D2	3 Peaks		
	['] Input: D3	4 Peaks		
NOTHING SELECTED SIZE	E: 81 x 59 TECH: schematic			(-77, 9)

Figure 24.4: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 2 and 3)

U Electric Eile Edit Cell Export Vi	iew Window Tools Help		-	- 0 ×
	• # 0.5 🗮 👎 🖪 🐚 💸 🗳 🕼 🔶 👄 🛥	•	- 4	5
				- 8 🗙
Explorer Layers	Ლ∏ 🛱 Panel 1 ∨ ग्रैंग 💠 ﷺ Ø H ◀ ■ ► H ▲ マ	Main: 4.894ns Cer Time Os		Ext: 4.894ns Center Delta: 0s 4ns 5ns 6ns 7ns 8ns 9ns
Bit Edit Cell Export View Yiew Simulation of 16-0-1-MuchCeT Export Layes If <	¹ Input: S3	× • • • • • • •	0	0
© D0 © D1 © D2 © D3	^² Input: S2	× □ ¥ ¥	1	1
	³ Input: S1	× 🗆)x())(0	0
+ D10 + D11 + D12 + D13	[•] Input: SO	× • • • • • • • • • • • • • • • • • • •	0	1
© D15 © S0 © S1 © S2	Output: Vo	ut 11 Peaks D	elay	Delay
Vout net@2 net@5 net@8	¦input: D4	5 Peaks		
	ⁱ Input: D5	6 Peaks		
NOTHING SELECTED SIZE	: 81 x 59 TECH: schematic			(-77, 9)

Figure 24.5: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 4 and 5)

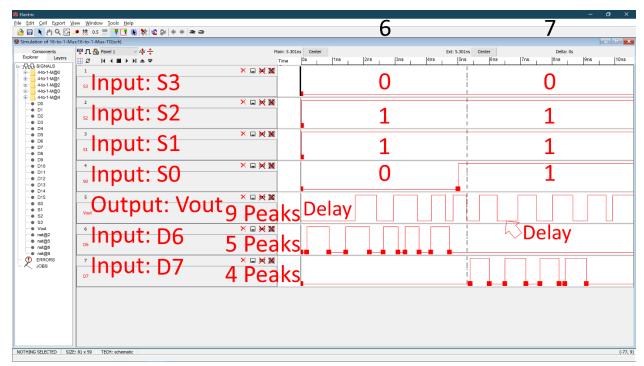


Figure 24.6: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 6 and 7)

			8	- ° ×
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Components Explorer Layers	₩ C H A B Panel 1 ↓ A ↓ A ↓ A ↓	Main: 5.213ns Time	Center s 1ns 2ns 3ns 4ns	Ext: 5.213ns Center Delta: 0s 6na 6ns 7ns 8ns 9ns 10ns
4-to-1-M@0 4-to-1-M@1 4-to-1-M@2 4-to-1-M@2	¹ Input: S3	× u ¥ ¥	1	1
Bile Edit Call Export Verv I Image: Simulation of the construction of the constru	^² Input: S2	× • ¥ ¥	0	0
D5 D6 D7 D8	³ Input: S1	× 🗆 💓 💥	0	0
+ D10 + D11 ++ D12 ++ D13	Input: SO	× 🗆 💥 💥	0	1
© D15 © S0 © S1 © S2	[*] Output: Vout	× □ × × 7 Peaks	Delay	
- 0 D4 - 0 D5 - 0 D5 - 0 D7 - 0 D9 - 0 D10 - 0 D11 - 0 D13 - 0 D13 - 0 D15 - 8 S1 - 8 S1 - 8 S1 - 8 S1 - 9 H15 - 9	I Donute DO	4 Peaks		Delay
ERRORS JOBS		3 Peaks		
NOTHING SELECTED SIZE	E: 81 x 59 TECH: schematic			(-77, 9)

Figure 24.7: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 8 and 9)

	iew Window Iools Help • 拱 0.5 ☴ 👎 🕇 💦 💸 🕸 🕼 🔶 👄 👄		10	- • ×
	nc16-to-1-Mux-TG(sch)	Main: 5.163ns	Center	Ext: 5.163ns Center Delta: 0s
Explorer Layers		Time	0s 1ns 2ns 3ns 4ns	Ex. 5.10/iii Center Dens. 05 5ns 6ns 7ns 8ns 9ns 10ns
4-to-1-M@0 4-to-1-M@1 4-to-1-M@2 4-to-1-M@2	¹ Input: S3	× 🖬 💥 💥	1	1
Elle Edit Cell Export Yjew Image: Standard of the standard of	² Input: S2	× 🖬 💓 💥	0	0
© D5 © D6 © D7 © D8	³ Input: S1	× u × x	1	1
+ D10 + D11 + D12 + D13	. Input: SO	X II X X	0	1
- © 05 - © 010 - © 010 - © 011 - © 012 - © 014 - ©	Output: Vou	t ^{× • × ×} 8 Peaks	Delay	Delay
	ໍຼີ Input: D10	4 Peaks		
- (I) ERRORS	Input: D11	4 Peaks		
NOTHING SELECTED SIZE	: 81 x 59 TECH: schematic			(-77, 9)

Figure 24.8: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 10 and 11)

😃 Electric			– 0 ×
		12	13
	≠ 恭 0.5 票 👎 🗄 🖹 📽 📽 🛊 🔶 👄 👄	12	
			- 7 🗙
		ns Center Ext: 4.762 Os 1ns 2ns 3ns 4ns	
E THE SIGNALS		Os Ins 2ns 3ns 4ns	5ns 6ns 7ns 8ns 9ns
Bit Cell Export Yew Simulation of 16-0-1-Murt 16 Commonts Export	s Input: S3	1	1
	² Input: S2	1	1
	^³ Input: S1 × ∞ × ∞ × ∞	0	0
D8	sinpacior		
© D10 © D11 © D12	¹ Input: S0 × □ × ∞ × ∞	0	1
	Output: Vout Peaks	Delay	Delay
- • 012 - • 013 - • 014 - • 015 - • 05 -	Input: D12 3 Peaks		
	input: D13 2 Peaks		
O 3 O 4 O 5 O 5 O 5 O 5 O 7 O 5 O 7 O 10			
NOTHING SELECTED SIZE	E: 81 x 59 TECH: schematic		(-77, 9)
-			

Figure 24.9: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 12 and 13)

🙂 Electric					– @ ×
			14		
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	ICT0-to-I-Mux-IG(SCN) 약 유규 즮 Panel 1 ···· 心 亽	Main: 4.819ns	Center	Ext: 4.819	
Bile Edit Cell Export View Yiew Simulation of 16-0-1-Mucc1-B File <		Time	Ds Ins Ins Ins	3ns 4ns	5ns 6ns 7ns 8ns 9ns
ie- 4-to-1-M@0	1	× 🗆 💓 💥			
4-to-1-M@2 4-to-1-M@3	Input: S3		_ 1		1
D0	2	× 🗆 💥 💥			
+ D2 + D3	Input: S2		1		1
	³ Input: S1	× 🗆 💓 💥	1		1
D8			_		±
- + D11	¹ Input: SO	× 🗆 💥 💥	0		1
D13	· ·				<u> </u>
\$ \$0 \$ \$1 \$ \$2	Cutput: Vou	t 4 Peaks	Delay		Delay
05 011 012 013 014 015 05 015 05 05 05 05 05 05 0	[•] Input: D14	1 Peak			
- () ERRORS	⁷ Input: D15	3 Peaks			
NOTHING SELECTED SIZE	: 81 x 59 TECH: schematic				(-77, 9)

Figure 24.10: IRSIM Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 14 and 15)

Section 5.2: Layout:

For the layout, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the selectors and counting the peaks for the one that's selected and comparing it with the output.

Electric e Edit Cell Export V	/iew Window Tools Help								- 0	
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Simulation of 16-to-1-M									- 1	9
Components	罕 🞵 🛗 Panel 1 🛛 🗸 🤹	Main: 4.55	5ns Center		Ext: 4.5			Delta: 0s		
Explorer Layers	≝₽ н∢∎⊁⊁≜⊽	Time	Os Ins	2ns 3n	s 4ns	5ns	6ns	7ns	8ns	
- + D0 - + D1	📩 Input: D0	×□×罴								
• D2	niput. D0	1 Peak								
D4										-
	² Input: D1									
	IIIpul. DI	2 Peaks	L				1	1	1	
	3						-		_	-
• D11	Input: D2									
D13	[™] mput. DZ	3 Peaks								
	4	× 🗆 💥 💥	1							
	Input: D3	1 Doole								
	" mpat. BS	4 Peaks						-• •-	<u> </u>	_
	5	🗙 🖂 🗡]					
- • net@6297	Input: D4	5 Peaks								
			<u>)</u>							_
net@6310 net@6314	- Innut DE	× • × ×								
 net@6315 net@6333 	Input: D5	6 Peaks								
• net@6339									-	-
• net@6349	⁷ Input: D6	E Doole								
net@6369	🛛 🖻 IIIput. Do	J PEAKS			1 1 1					
 e net@6383 e net@6385 	8	× 🖬 💥 💥								-
 net@6395 net@6404 	Input: D7	4 Peaks								
	mpat. D7	TICUNS								
• net@6429	° • • • • •	× □ × ¥								_
- • net@6566	Input: D8	4 Peaks								
• net@6576 🧠					<u> </u>					
OTHING SELECTED SIZ	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MO	515)							(-170.5	5,

Figure 25.1: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer

lation of 16-to-1-Mu	• 弗 0.5 荒 👎 📑 🐚 💸 🗳 🕼 🔶 👄 👄		
Components	[16-to-i-Mux(lay) [[] 月 高 Panel 1 · · · 心 초	Main: 4.555ns Center E	Ext: 4.555ns Center Delta: 0s
orer Layers		Time 0s 1ns 2ns 3ns 4ns	
SIGNALS ^	8	べ Ⅲ 舛 渡	
 D1 D2 D3 	Input: D7	4 Peaks	
D4 D5	9	× • × ¥	
 D5 D6 D7 D8 	Input: D8	4 Peaks	
 D9 D10 	10	× 🗆 💓 💥	
 D11 D12 D13 	Input: D9	3 Peaks	
 D14 D15 	11		
 \$0 \$1 \$2 	DID Input: D10	4 Peaks	
 S3 Vout net@6293 	¹² Input: D11		
 net@6297 net@6303 		4 Peaks	
 net@6304 net@6310 net@6314 net@6315 	¹³ Input: D12	3 Peaks	
net@6333	•		i
 net@6339 net@6340 net@6349 net@6360 	¹⁴ Input: D13	2 Peaks	
 net@6369 net@6383 			
 net@6385 net@6395 net@6404 net@6413 	¹⁵ Input: D14	1 Peak	
 net@6413 net@6420 net@6429 net@6436 	¹⁶ Input: D15		
● net@6566 ● net@6576		JEANS	

Figure 25.2: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer

🙂 Electric				– 61 ×
	/iew Window Tools Help ノチ 拱 0.5 読 👎 📑 🐚 💸 🗳 😭 🔶 👄 👄		0	1
Simulation of 16-to-1-Mi			U	- 8 ×
Components Explorer Layers	थि प वि Panel 17 v ntr 🛧 ∰ 8 र र र ∎ ► H A マ	Main: 5.001ns Time	Center Ext: 5.001 Os 1ns 2ns 3ns 4ns	ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns
• D0 • D1 • D2 • D3	[™] Input: S3	× 🖬 💓 💥	0	0
	[™] Input: S2	× 🗆 💥 💥	0	0
	^a Input: S1	× □ 涎 涎	0	0
D14 D15 S0 S1 S2	²⁰ Input: SO	× 🖬 💥 💥	0	1
	²¹ Output: Vout	× □×× 3 Peaks	Delay	Delay
 netg6310 netg6314 netg6315 netg6333 netg6339 	["] Input: D0	1 Peak		
 net@6340 net@6349 net@6360 net@6360 net@6369 net@6363 	^a Input: D1	2 Peaks		
• net@6385 • net@6395 • net@6404 • net@6413				
e net@6420 e net@6429 e net@6436 e net@6566 e net@6576 v				
	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-170.5, 161.5)

Figure 25.3: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 0 and 1)

😲 Electric				- 6 X
File Edit Cell Export Vi	iew Window Tools Help • 拱 0.5 蒜 👎 👎 🐚 💸 📽 😭 🔶 👄 👄		2	3
Simulation of 16-to-1-Mu	nc16-to-1-Mux{lay}		_	- 8 ×
Components Explorer Layers	罕几品 Panel 1 → 办☆ ※ 경 내 ◀ ■ ▶ 위 ▲ マ	Main: 5.033ns Time	Center Ext: 5.03 Os Ins 2ns 3ns 4ns	Sins Delta: 0s 5ns 6ns 7ns 8ns 9ns 1
	¹ Input: S3	× 🖬 💥 💥	0	0
© D4 © D5 © D6 © D7 © D8	² Input: S2	× 🗆 🗙 🐹	0	0
	³ Input: S1	¥ ¥ ¥ ×	1	1
+ D14 + D15 + S0 + S1 + S2	Jinput: SO	× 🗆 💥 💥	0	1
	[•] Output: Vou	t 7 Peaks	Delay	Delay
 net@6310 net@6314 net@6315 net@6333 net@6333 	[•] ₂ Input: D2	3 Peaks		
 net@6340 net@6349 net@6360 net@6369 net@6363 	['] _Input: D3	4 Peaks		
net@6385 net@6395 net@6404 net@6413				
+ net@6420 + net@6429 + net@6436 + net@6566 + net@6576				
NOTHING SELECTED SIZE	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-170.5, 161.5)

Figure 25.4: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 2 and 3)

😲 Electric			-	- 0 ×
	iew Window Tools Help • # 0.5 🗮 👎 🔁 🐚 💸 🗳 🕼 🔶 👄		4	5
Simulation of 16-to-1-Mu				
Components Explorer Layers	ײִ <u>1</u> 🛱 Panel 1 → nो 🛧 ∰ अग्र 1 🖬 → M 🔺 🗢	Main: 4.894ns Time	Center s Ins 2ns 3ns	Ext: 4,894ns Center Delta: 0s 4ns 5ns 6ns 7ns 8ns 9ns
	¹ Input: S3	× • • • • ×	0	0
D4 D5 D6 D7 D8	^² Input: S2	× • × × ×	1	1
D9 D10 D11 D12 D13	³ Input: S1	× 🗆 💓 💥	0	0
D14 D15 S0 S1 S2	[•] Input: SO	× □ ※ 鯊	0	1
 S3 Vout net@6293 net@6297 net@6303 net@6304 	Output: Vou	ıt × ∞×× 11 Peaks	Delay	
 net@6310 net@6314 net@6315 net@6333 net@6333 	¦Input: D4	5 Peaks		
 net@6340 net@6349 net@6360 net@6360 net@6369 net@6383 	ⁱ Input: D5	6 Peaks		
• net@6385 • net@6395 • net@6404 • net@6413				
 net@6420 net@6429 net@6436 net@6566 net@6566 net@6576 				
NOTHING SELECTED SIZE	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-170.5, 161.

Figure 25.5: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 4 and 5)

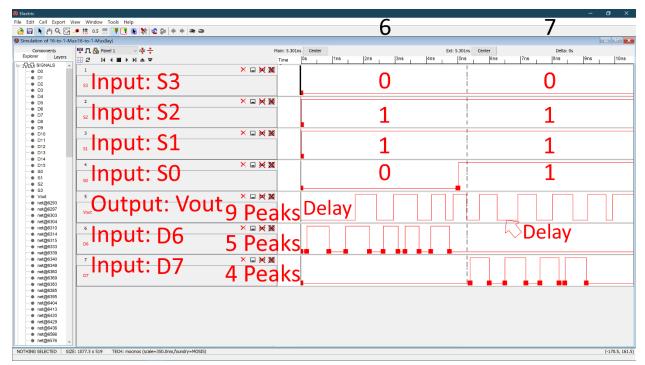


Figure 25.6: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 6 and 7)

💭 Electric			<u> </u>	- 0 ×
	'iew Window Tools Help 🏓 👯 0.5 👯 👎 🔁 🐚 💸 📽 😩 🖨 🖨 👄		8	9
Dimulation of 16-to-1-Mu				- 8 ×
Components Explorer Layers	罕几品 Panel 1 → ∲ ∻ Ⅲ 2	Main: 5.213ns Center Time Os	Ins 2ns 3ns 4ns	Ext: 5.213ms Center Delta: 0s jóna jéna 7ns 8ns 9ns 10ns
00 01 02 03 04	¹ Input: S3	× □	1	1
	² Input: S2	× 🖬 💥 💥	0	0
© D9 © D10 © D11 © D12 © D13	³ Input: S1	×□涎涎	0	0
D14 D15 S0 S1 S2	Input: SO	× • ¥ X	0	1
 \$3 Vout net@6293 net@6297 net@6303 net@6304 	Cutput: Vou	t 7 Peaks De	elay	
• net@6310 • net@6314 • net@6315 • net@6333 • net@6339	🕯 Input: D8	4 Peaks		Delay
net@6349 net@6360 net@6369 net@6369 net@6369 net@6363	ⁱ Input: D9	3 Peaks		
 net@6385 net@6395 net@6404 net@6413 				
NOTHING SELECTED SIZE	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-170.5, 161.5

Figure 25.7: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 8 and 9)

😟 Electric File Edit Cell Export Vi	iew Window Tools Help		10	- ° ×
👌 🗟 📐 🖑 Q 🐼 -	🍠 拱 0.5 蒜 📑 📑 💽 💸 🗳 🎥 🔶 👄 🧼		10	
Simulation of 16-to-1-Mu	Inc16-to-1-Mux{lay} □ □ □ 1 □ 1 □ 1 □ 1 □ 1 □ 1 □ 1 □ 1 □	Main: 5.163ns	Center Ext:	5.163ns Center Delta: 0s
Components Explorer Layers		Time	Center Ext: 0s 1ns 2ns 3ns 4ns	5.163ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns 10ns
	^₁ Input: S3	× 🗆 💥 🐹	1	1
04 05 06 07 08	² Input: S2	× = × ¥	0	0
09 010 011 012 013	s. Input: S1	× 🗆 💥 🐹	1	1
© D14 © D15 © S0 © S1 © S2	Input: SO	× 🗆 💥 💥	0	1
	[•] Output: Vou	t 8 Peaks	Delay	Delay
 net@6310 net@6314 net@6315 net@6333 net@6339 	ຼໍມInput: D10	4 Peaks		
net@6340 net@6349 net@6360 net@6369 net@6369 net@6363	['] Input: D11	4 Peaks		
net@6385 net@6395 net@6404 net@6413				
net@6420 net@6429 net@6438 net@6566 net@6576				
NOTHING SELECTED SIZE	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-170.5, 161.5)

Figure 25.8: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 10 and 11)

😨 Electric				– 0 ×
File Edit Cell Export Vi			12	13
	• 恭 0.5 微 👎 🔁 🐧 🛸 🗳 🖗 + 🔿 👄 👘		12	
Simulation of 16-to-1-Mu				- # 🗙
Components Explorer Lavers	🕎 🎵 🛗 Panel 1 🛛 🗸 🕸	Main: 4.762ns		
SIGNALS ^	≝₿ н∢∎≻н≜⊽	Time	0s 1ns 2ns 3ns 4ns	5ns 6ns 7ns 8ns 9ns
- • D0 - • D1		× □ ⋈ Ж		
- • D2	Input: S3		1	1
• D3	- mpacioo			· -
- + D5	2	× 🗆 💥 麗	_	-
	Input: S2		1	1
D8				· · · · · · · · · · · · · · · · · · ·
	3	× 🗆 💥 💥		
- + D11	¹ Input: S1		0	
+ D12 + D13	sinput. Jr			V
	4	× 🗆 💥 💥		
- • S0	Input: SO		0	1
\$ \$1 \$ \$2	sinput. 50		U	
- • S3				
	<u>⊢`Outout∙ \/ou</u>			Delevi
	Output: Vou	5 Peaks	Delav	Delay
 net@6304 				
net@6310 net@6314	Input: D12	× 🗆 💥 💥		
		3 Peaks		
	· · ·		• • • • • • •	1
 net@6340 net@6349 	input: D13	2 Peaks		
• net@6360	minput. DT2	2 Peaks		
	013			
- • net@6385				
net@6413				
- • net@6436				
net@6566 net@6576				
NOTHING SELECTED SIZE	: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-170.5, 161.5)
				()

Figure 25.9: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 12 and 13)

😃 Electric					- 0 ×
File Edit Cell Export V	iew Window Tools Help 🧈 拱 0.5 👯 👎 🎦 💦 💸 🙋 🕼 🔶 👄 👄		14		- 15
Simulation of 16-to-1-Mu					- 7 🗙
Components Explorer Layers	罕 ∏ 🛱 Panel 1 → 🛝 💠 ⅲ ८ । । । ■ ►) । ▲ 🗢	Main: 4.819ns Time	Center Os 1ns 2ns 3ns	Ext: 4.819ns Center	Delta: 0s 6ns 7ns 8ns 9ns
	¹ Input: S3	× 🖬 💥 💥	. 1		1
	^² Input: S2	× 🗆 💥 💥	1		1
09 010 011 013 014	³ Input: S1	× 🖬 💓 💥	1		1
	[•] Input: SO	× 🖬 💥 💥	0		1
\$ \$3 \$ Vout \$ net@6293 \$ net@6297 \$ net@6303 \$ net@6304	[*] Output: Vou	t 4 Peaks	Delay	De	lay
net@6310 net@6314 net@6315 net@6333 net@6339	input: D14	× ■ × × × × × 1 Peak			
 net@6340 net@6349 net@6360 net@6369 net@6369 	⁷ Input: D15	3 Peaks			
net@6385 net@6395 net@6404 net@6413					
 net@6420 net@6429 net@6436 net@6566 net@6566 					
	E: 1077.5 x 519 TECH: mocmos (scale=350.0nm,foundry=MOSIS)				(-170.5, 161.5)

Figure 25.10: IRSIM Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Selector at 14 and 15)

😍 Electric							- 0 ×
Eile Edit Cell Export Vi							
🚵 🖬 📐 🖑 📿 -	• 井 0.5 🇮 👎 📑 🐚 💸 🗳 🕼 🔶 👄	3					- 8 ×
	crie-to-I-Mux-IG(ay) 罕几晶 Panel 1 ~ 載 🍫	Main: 4 FF	ins Center		Ext: 4.555ns Center	Delta: 0	
Explorer Layers		Time	los Ins	2ns 3ns	4ns 5ns	6ns 7ns	8 8ns , 9r
	¹ Input: D0	× ¤×× 1 Peak					^
 D5 D6 D7 D8 D9 	² Input: D1	2 Peaks	P				
	³ Input: D2	3 Peaks					
+ D15 + S0 + S1 + S2 + S3	Input: D3	4 Peaks					
 Vout net@909 net@930 net@931 net@952 	^₅ Input: D4	5 Peaks					
net@1090 net@1111 net@1112 net@1143	ⁱ Input: D5	6 Peaks					
 net@1144 net@1271 net@1273 net@1276 net@1327 	⁷ Input: D6	5 Peaks					
 net@1360 net@1381 net@1382 net@1413 net@1414 	[*] Input: D7	4 Peaks					
• net@1594 • net@1632 • net@1637 • net@1644 v		4 Peaks					v
NOTHING SELECTED SIZE	: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=1	(OSIS)					(-859, 181)

Figure 26.1: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer

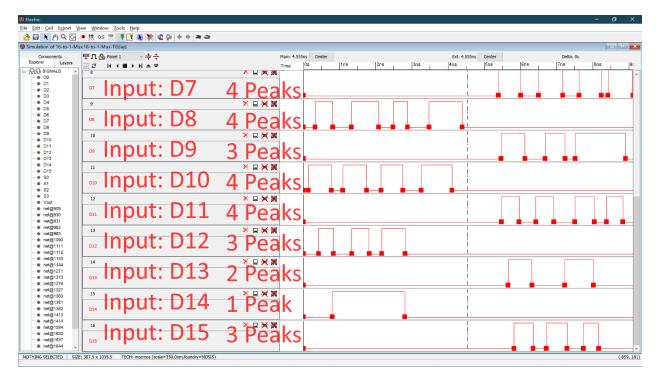


Figure 26.2: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer

😟 Electric				- 6 ×
	(jew Window Iools Help ● 拱 0.5 👎 📑 🐚 💸 📽 🕼 🔶 👄 👄		0	1
Simulation of 16-to-1-Mit			•	- 8 ×
Components Explorer Layers	Ლ几品 Panel 17 ∨ ग्री ∻ ﷺ ८ । । र ∎ ►) । ▲ マ	Main: 5.001ns Time	Center Ext: 5.002 Cs 1ns 2ns 3ns 4ns	ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns
• D0 • D1 • D2 • D3	["] Input: S3	× 🖬 💓 💥	0	0
	[™] Input: S2	× 🗆 💥 💥	0	0
	¹ Input: S1	×□∑≋	0	0
D14 D15 S0 S1 S2	²⁰ Input: SO	× 🖬 💥 💥	0	1
	²¹ Output: Vout	× • × × × × × × × × × × × × × × × × × ×	Delay	Delay
 net@002 net@1090 net@1111 net@1112 net@1143 	² Input: D0	1 Peak		
 net@1144 net@1271 net@1273 net@1276 net@1327 	²³ Input: D1	2 Peaks		
• net@1360 • net@1381 • net@1382 • net@1382				
e net@1414 e net@1594 e net@1632 e net@1637 e net@1644				
NOTHING SELECTED SIZ	E: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-859, 181)

Figure 26.3: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 0 and 1)

😃 Electric				- 0 ×
Eile Edit Cell Export Vi	ew Window Iools Help • # 0.5 # 👎 📑 🕟 🔆 🕸 😭 + 🔿 👄		2	3
📴 🖬 🥂 🖑 🗠 -			Z	J
Components Explorer Layers	Ლ几冊 Panel 1 ✓ ग्रै ∻ Ⅲ Ø N 4 ■ → N ▲ マ	Main: 5.033ns Time	Center Ext: 5.03 Os 1ns 2ns 3ns 4ns	
00 	¹ Input: S3	× • • ¥	0	0
	^² Input: S2	× • ¥	0	0
	input: S1	× 🗆 💓 💥	1	1
	Jinput: SO	× 🗆 💥 🐹	0	1
Vout • Vout • net@909 • net@930 • net@931	Cutput: Vou	^{× ••} ×× 7 Peaks	Delay	Delay
• netgot2 • e netgot3 • e netg0090 • e netg01111 • e netg01112 • e netg01143	[°] Input: D2	3 Peaks		
- et@1144 - et@1271 - et@1273 - et@1276 - et@1327	['] Input: D3	[×] • × ∗ × × 4 Peaks		
net@1360 net@1381 net@1382 net@1413 net@1414				
• net@1594 •• net@1594 •• net@1632 •• net@1637 •• net@1644 v				
NOTHING SELECTED SIZE	387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-859, 181)

Figure 26.4: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 2 and 3)

😨 Electric Eile Edit Cell Export V	view Window Iools Help		-	- 6 ×
	→ ∰ 0.5 ∰ <mark>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 </mark>		4	5
Simulation of 16-to-1-Mi Components	lux:16-to-1-Mux-TG(lay) 罕几品 Panel 1 √ 载 李	Main: 4.894ns	Center	Ext: 4.894ns Center Delta: 0s
Explorer Layers	III 2 N I I ► N ▲ ▼	Main: 4.894ns		Ext: 4.894ns Center Delta: 0s
	[™] Input: S3	× 🗆 💥 💥	0	0
	^² Input: S2	× • ¥ ¥	1	1
D10 D11 D12 D13 D14	input: S1	× 🖬 💥 💥	0	0
D15 S0 S1 S2 S3	[•] Input: SO	× 🗆 💥 💥	0	1
Vout • vout • net@909 • net@930 • net@931 • net@952	့်Output: Voi	L L Cav2⊢	Delay	Delay
 net@963 net@1090 net@1111 net@1112 net@1143 	¦nput: D4	× ■ × × × × × × × × × × × × × × × × × ×		
 net@1144 net@1271 net@1273 net@1276 net@1327 	[*] Input: D5	6 Peaks		
 net@1360 net@1381 net@1382 net@1413 net@1414 				
• net@1594 • net@1594 • net@1632 • net@1637 • net@1644 v				
NOTHING SELECTED SIZ	E: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)		(-859, 181)

Figure 26.5: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 4 and 5)

😃 Electric					- 0 ×
Eile Edit Cell Export Vi	jew Window Iools Help ● 拱 0.5 読 👎 👎 限 💸 🕸 😭 🔶 👄 👄		6		7
Simulation of 16-to-1-Mu			0		- # 🗙
Components Explorer Layers	罕几品 Panel 1 → 心 ⁴ ~ ※ 2 H イ ■ ト H ▲ マ	Main: 5.301ns Time	Center Ins 2ns 3ns 4ns	Ext: 5.301ns Center 5ns 6ns 7ns	Delta: 0s 8ns 9ns 10ns
D0 0 0 0 0 0 0 0	Input: S3	× • ¥ ¥	0		0
	^² Input: S2	× • ¥	1		1
• 010 • 011 • 012 • 013 • 014	Înput: S1	× • • • • • • •	1		1
• 511 • • 50 • • \$1 • • \$2 • • \$3	Input: SO	× • ¥ ¥	0		1
Vout 	Cutput: Vou	[×] [×] [×] [×] 9 Peaks	Delay		
• netgot2 • e netgot3 • e netg0090 • e netg01111 • e netg01112 • e netg01143	[∴] Input: D6	5 Peaks			elay
• net@1144 •• net@1271 •• net@1273 •• net@1276 •• net@1327	['] _" Input: D7	4 Peaks			
• net@1360 • net@1381 • net@1382 • net@1382					
+ net@1414 + net@1594 + net@1632 + net@1637 + net@1644					
NOTHING SELECTED SIZE	E: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)				(-859, 181)

Figure 26.6: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 6 and 7)

😕 Electric Eile Edit <u>C</u> ell Export V	ijew <u>W</u> indow <u>I</u> ools <u>H</u> elp		0	- ° ×
	🔎 拱 0.5 拱 📑 🔁 🐧 💸 📽 🕼 🔶 👄 👄		8	9
Simulation of 16-to-1-Mi				- 🕫 🗙
Components Explorer Layers	थि nel 1 ∨ n‡r + + + + + + + + + + + + + + + + + + +	Main: 5.213ns Ce Time Os	Ins 2ns 3ns 4ns	Ext: 5.213ns Center Delta: 0s 5ns 6ns 7ns 8ns 9ns 10ns
• • D0 • • D1 • • D2 • • D3 • • D4	¹ Input: S3		1	1
© D5 © D6 © D7 © D8	^² Input: S2	× • × ×	0	0
+ D9 + D10 + D11 + D12 + D13	³ Input: S1		0	0
D14 D15 \$ \$0 \$ \$1 \$ \$2	🖫 Input: SO	× 🗆 💥 💥	0	1
 S3 Vout net@909 net@930 net@931 net@962 	Cutput: Vou	^t 7 Peaks D)elay	
 net@02 net@1090 net@1111 net@1112 net@1143 	^{Input: D8}	4 Peaks		Delay
net@1144 net@1271 net@1273 net@1276 net@1327	ⁱ Input: D9	3 Peaks		
• net@1360 • net@1381 • net@1382 • net@1382				
net@1414 net@1594 net@1632 net@1637 net@1644				
NOTHING SELECTED SIZ	E: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-859, 181)

Figure 26.7: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 8 and 9)

Electric File Edit Cell Export V	iew Window Iools Help • # 0.5 🛒 👎 🔁 💦 💸 🕸 🕼 🔶 👄 👄		10	- ° ×
Simulation of 16-to-1-Mu			10	- 8 🗙
Components Explorer Layers	₩ <u>Π</u> Banel 1 ↓ ψr ÷ ∰ Ø N I I ► N A ▼	Time	Center 2ns 3ns 4m	Ext: 5.163ns Center Delta: 0s : 5ns 6ns 7ns 8ns 9ns 10ns
	¹ Input: S3	× u 💥 💥	1	1
	² Input: S2	× • ¥ ¥	0	0
010 011 012 013 014	Input: S1	× u 💥 💥	1	1
© D15 © S0 © S1 © S2	. Input: SO	派 河 二 ×	0	1
+ S3 + Vout + net@909 + net@930 + net@931 + net@962	Output: Vou	t × • × × × × × × × × × × × × × × × × ×	Delay	Delay
• net@02 • e net@053 • e net@1090 • et@1111 • e net@1112 • e net@1143	ຼົມInput: D10	4 Peaks		
• net@1144 ••• net@1271 ••• net@1273 ••• net@1276 ••• net@1327	Input: D11	4 Peaks		
 net@1360 net@1381 net@1382 net@1413 net@1414 				
• net@1594 ••• net@1594 ••• net@1632 ••• net@1637 ••• net@1644				
NOTHING SELECTED SIZE	: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)			(-859, 181)

Figure 26.8: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 10 and 11)

😃 Electric						- 0 ×
<u>Eile Edit Cell Export V</u>			12		13	2
	≠ 恭 □5 読 👎 🖪 🐧 💸 🗳 😭 🔶 希 🏔				<u> </u>	
Simulation of 16-to-1-Mu						- # ×
Components Explorer Lavers	🕎 Π 📇 Panel 1 🛛 🗸 📌	Main: 4.762ns		Ext: 4.762n		Delta: 0s
E Jun Signals	≝₿ н∢∎⊁н≜⊽	Time	Os Ins 2ns	3ns 4ns	5ns 6ns 7r	is 8ns 9ns
- + D0		× 🗆 💥 🐹				
- + D2	Input: S3		1	1	1	
- • D3			· · · ·	1		-
D5	2	🗙 🗆 💥 麗				
	Input: S2		1		1	
- • D8	* mpat. 52			i	-	-
+ D9 + D10	3	× 🗆 💓 💥		1	-	
+ D11 + D12	¹ Input: S1		0		(
+ D13	simput. 5±					
	1	× ⊑ ¥ ¥				
• S0 • S1	Input: SO		0			
- • S2	s input. 50		, v	1	1 1	
- • \$3	5	X 🗆 🖌 💥				
net@909	Output Vout		Dolou		Delay	
net@930 net@931	Cutput: Vout	5 Peaks	Delay		Delay	
 net@962 net@963 		× ⊑ ¥ ¥			f	
- • net@1090	Input: D12					
 net@1111 net@1112 		3 Peaks				
• net@1143						
• et@1144 • et@1271	<u>Input: D13</u>					
 net@1273 net@1276 		2 Peaks		i		
net@1327				I	i	• •
• net@1360 • ent@1381						
net@1382						
net@1413 net@1414						
• net@1594						
et@1637						
• net@1644 v						
NOTHING SELECTED SIZE	: 387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)					(-859, 181)

Figure 26.9: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 12 and 13)

😃 Electric				- 0	ı x
<u>Eile E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u> i			14	15	
🚵 🖬 📐 🖑 🛇 -			<u>14</u>		
Simulation of 16-to-1-Mu	1				e 🗙
Components Explorer Lavers	🕎 🎵 🛗 Panel 1 💎 🕸	Main: 4.819ns		Ext: 4.819ns Center Delta: 0s 4ns 5ns 6ns 7ns 8ns	9na
SIGNALS A	ⅲ♂ н∢∎⊁н≜⊽	Time	Os Ins 2ns 3ns	4ns 5ns 6ns 7ns 8ns	3115
	^{Input:} S3	× 🖬 💥 💥	. 1	1	
	^² Input: S2	× 🗆 💥 💥	1	1	
	Input: S1	× 🗆 💓 💥	1	1	
© D14 © D15 © S0 © S1 © S2 © S3	Jinput: SO	× 🗆 💥 🐹	0	1	
● Vout ● Vout ● net@909 ● net@930 ● net@931	[*] Output: Vou	t 4 Peaks	Delay	Delay	
• netgo1112 • • netg01112 • • netg01112	Input: D14	1 Peak			
 net@1144 net@1271 net@1273 net@1276 net@1327 	Input: D15	3 Peaks			
NOTHING SELECTED SIZE	387.5 x 1035.5 TECH: mocmos (scale=350.0nm,foundry=MOSIS)				(-859, 181)

Figure 26.10: IRSIM Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Selector at 14 and 15)

Section 5.3: Comparison:

For IRSIM, by comparing Figure 23 (Conventional Schematic), Figure 24 (Transmission Gate Schematic), Figure 25 (Conventional Layout), and Figure 26 (Transmission Gate Layout) with each other, the way the output reacted given the certain inputs appears to be the same. In addition, with the inputs we gave, it gave us the appropriate outputs that we were looking for, so it confirms that our design is correct. The outputs that we were looking from could be seen by using the truth table on Table 1. The only noticeable difference between the figures would be the propagation delay, which could be seen on Table 6. Depending on the which design, each has its own different propagation delay.

In conclusion, IRSIM shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time, and propagation delay. The differences can be viewed on Table 6, which has a summary of the measurements.

Section 6: LTSPICE Code and Parasitic Extractions:

The Spice Code that we wrote is shown on Figure 27. It provides certain values to the inputs so that it'll be able to produce a certain output. The computations that we tested set each input (D0-D15) high for 50 nanoseconds at different times, then back to low; in other words, 100 nanoseconds period, with rise time and fall time of 5 nanoseconds and 50% duty cycle. Each of the inputs were high at different times so they wouldn't be able to relate to each other. After that, we set tested all the computations for the selector (S0-S3), starting from 0 to 15. This way, it'll be able to output each individual input and show a wavelike output.

We ran LTSPICE on the conventional 16-to-1 Multiplexer Schematic, conventional 16to-1 Multiplexer Layout, transmission gate 16-to-1 Multiplexer Schematic, and transmission gate 16-to-1 Multiplexer Layout and it generated a code underneath it. A sample of the Spice Deck and Parasitic Extractions that came from those designs are shown from Figure 28 to Figure 35.

VDD VDD 0 DC 3.3 VGND GND 0 DC 0 Vin2 D0 0 PULSE (0 3.3 0n 5n 5n 50n 1600n) Vin3 D1 0 PULSE (0 3.3 100n 5n 5n 50n 1600n) Vin4 D2 0 PULSE (0 3.3 200n 5n 5n 50n 1600n) Vin5 D3 0 PULSE (0 3.3 300n 5n 5n 50n 1600n) Vin6 D4 0 PULSE (0 3.3 400n 5n 5n 50n 1600n) Vin7 D5 0 PULSE (0 3.3 500n 5n 5n 50n 1600n) Vin8 D6 0 PULSE (0 3.3 600n 5n 5n 50n 1600n) Vin9 D7 0 PULSE (0 3.3 700n 5n 5n 50n 1600n) Vin10 D8 0 PULSE (0 3.3 800n 5n 5n 50n 1600n) Vin11 D9 0 PULSE (0 3.3 1000n 5n 5n 50n 1600n) Vin12 D10 0 PULSE (0 3.3 1000n 5n 5n 50n 1600n) Vin13 D11 0 PULSE (0 3.3 1200n 5n 5n 50n 1600n) Vin14 D12 0 PULSE (0 3.3 1200n 5n 5n 50n 1600n) Vin15 D13 0 PULSE (0 3.3 1200n 5n 5n 50n 1600n) Vin16 D14 0 PULSE (0 3.3 1500n 5n 5n 50n 1600n) Vin17 D15 0 PULSE (0 3.3 100n 5n 5n 50n 1600n) Vin18 S0 0 PULSE (0 3.3 100n 5n 5n 50n 1600n) Vin19 S1 0 PULSE (0 3.3 100n 5n 5n 50n 1600n) Vin19 S1 0 PULSE (0 3.3 400n 5n 5n 400n 800n) Vin20 S2 0 PULSE (0 3.3 800n 5n 5n 50n 1600n)

Figure 27: Spice Code Written For LTSPICE

🦅 Utrpice XVII = [16-to-1-Mux.spi]	 ٥	×
🖹 File Edit View Simulate Iools Window Help		8 x
▶■■ 型体ののの気障は国家をある時間の「なっている」をついていたのです。		
B 18-to-1-Mux spi = 18-to-1-Mux spi		
<pre>*** SPICE deck for cell 16-to-1-Mux(sch) from library 16-to-1-Mux *** Created on Tue Oct 29, 2019 15:40:18 *** Last revised on Sun Nov 09, 2019 10:46:45 *** Written on Sun Nov 10, 2019 14:19:50 by Electric VLSI Design System, version 9.07 *** Layout tech: mocmos, foundry MOSIS *** UC SPICE *** , MIN.RESIST 4.0, MIM_CAPAC 0.1FF</pre>		^
*** SUBCIRCUIT 16-Lo-1-Mux_AND FROM CELL AND[sch] .SUBCKT_16-to-1-Mux_AND A B Vout ** GLOBAL gnd ** GLOBAL gnd ** GLOBAL vdd Mnmos82 net810 B gnd gnd NMOS L-0.35U W-0.075U Mnmos82 vout net812 A und gnd gnd NMOS L-0.35U W-0.875U Mpmos81 vdd B net812, vdd PMOS L-0.35U W-1.75U Mpmos82 vdd B net812, vdd PMOS L-0.35U W-1.75U Mpmos82 vdd B net812, vdd PMOS L-0.35U W-1.75U Mpmos82 vdd net812, Vout vdd PMOS L-0.35U W-1.75U		
*** SUBCIECUIT 16-to-1-Mux_3-AND FROM CELL 3-AND(sch) *SUBCKT_16-to-1-Mux_3-AND A B C Vout ** GLOBAL vdd ** GLOBAL vdd XAND00 h B nct00_16-to-1-Mux_AND XAND01 nct00_C Vout_16-to-1-Mux_AND XAND01 nct00_C Vout_16-to-1-Mux_AND XAND01 nct00_C Vout_16-to-1-Mux_AND XAND01 nct00_C Vout_3-AND		ł
*** SUBCIRCUIT 16-to-1-Mux OR FROM CELL OR(sch) .SUBCKT 16-to-1-Mux OR A Wout. ** GLOBAL Vdd Mnmos80 vout nct813 gnd gnd NMOS L-0.35U W-0.875U Mnmos81 nct813 gnd gnd NMOS L-0.35U W-0.875U Mnmos82 ret813 g nd gnd NMOS L-0.35U W-0.875U Mpmos80 vdd A nct82 vdd PMOS L-0.35U W-1.75U Mpmos80 vdd A nct82 vdd PMOS L-0.35U W-1.75U Mpmos82 vdd nct82 Notl vdd PMOS L-0.35U W-1.75U Mpmos82 vdd nct813 vdd PMOS L-0.35U W-1.75U		
*** SUBCIRCUIT 16-to-1-Mux 4-OR FROM CELL 4-OR(sch) .SUBCKT 16-to-1-Mux 4-OR FROM CELL 4-OR(sch) ** GLOBAL gnd ** GLOBAL gnd ** GLOBAL net89 16-to-1-Mux_OR XOR80 A B net89 16-to-1-Mux_OR XOR81 net89 16-to-1-Mux_OR XOR82 C D net89 16-to-1-Mux_OR XOR82 C D net89 16-to-1-Mux_OR XOR82 C D net89 16-to-1-Mux_OR XOR82 C D net89 16-to-1-Mux_OR		~

Figure 28: Generated Spice Deck of Conventional 16-to-1 Multiplexer Schematic

⁷ (Tripice XVII - 116-to-11-Muxsa)] − 0 ⁷ X
■ Efe Edit Vew Simulate Tools Window Help - ・ * ●
*** SPICE deck for cell 16-to-1-Mux(1ay) from library 16-to-1-Mux *
*** Last revised on Sat Nov 09, 2019 10:46:51
*** Written on Sun Nov 10, 2019 14:16:37 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
*** P-Active: areacape.9Ff/um22_edgecape0.0Ff/um, res=2.5ohms/gg
*** N-Active: areacap=0.9Ff/um ² , edgecap=0.0Ff/um, res=3.0ohms/sq *** Polysilicon=1: areacap=0.16fFf/um ² , edgecap=0.060Ff/um, res=6.2ohms/sq
*** Polysilicon-2: areacap=1.0Ff/um ² , edgecap=0.0Ff/um, res=50.0ohms/sq
*** Transistor-Poly: areacap=0.09FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sg
*** Poly-Cut: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=2.20hms/sq
*** Active-Cut: areacap=0.0FF/um2, edgecap=0.0FF/um, res=2.5ohms/ag *** Mctal: research 2/20FE/um2, edgecap=0.10FF/um, res=0.078chme/ag
Metal-1. aleacap-0.1203FF/dm 2, edgecap=0.1104FF/dm, les=0.0700fmms/sq
*** Vial: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sg *** Metal-2: areacap=0.08FF/um^2, edgecap=0.09FF/rum, res=0.078ohms/sg
*** Via: areacape.ord/F/um2, edgecape.org/Afr/um, resel.90hms/sq
*** Metal-3: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq
*** Via3: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq
*** Metal-4: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq
*** Vi4: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq *** Meta15: areacap=0.0815F/um^2, edgecap=0.0FF/um, res=0.0780hms/sq
*** Metal-5: areacap=0.0843FF/um ² , edgecap=0.0974FF/um, res=0.0700hms/sq *** Via5: areacap=0.0FF/um ² 2, edgecap=0.0FF/um, res=0.80hms/sq
*** Metal-6: areacap=0.0423F/um2, edgecap=0.1273F/um, res=0.036ohms/sq
*** Hi-Res: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sq
*** TOP LEVEL CELL: 16-to-1-Mux(lav)
Mnmos0460 gnd net06395 net06310 gnd NMOS L=0.350 W=1.750 AS=1.378P AD=6.931P PS=3.6750 PD=17.0680
Mnmos@461 net@6310 net@6297#6nmos@461_poly-left gnd gnd NMOS L=0.35U W=1.75U AS=6.931P AD=1.378P PS=17.068U PD=3.675U
Mnmos@462 net@6369 net@6310#13nmos@462_poly-right gnd gnd NNOS L=0.35U W=1.75U AS=6.931P AD=1.991P PS=17.068U PD=5.775U
Mmmos#463 gnd net@633344nmos#463_poly-left net@6310 gnd NMOS L=0.35U W=1.75U AS=1.378P AD=6.931P PS=3.675U PD=17.068U Mmmos#464 net@6310 net@640442Pmmos#464 poly-left nnd qnd NMOS L=0.35U W=1.75U AS=6.931P AD=1.378P PS=1.7068U PD
mmoseve necesso necesso provente una porver una dia mos necesso wellisto necesso realisto realisto realisto realisto de la solo
Mmmosd466 net@65666 net@6560#18nmosd466 poly-left net@6576 qnd NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos@467 net@6395#3contact@2359 metal=1-polysilicon-1 net@6293#2nmos@467 poly-right gnd gnd NMOS L=0.350 W=1.750 AS=6.931P AD=1.991P PS=17.0680 PD=5.7750
Mnmos@468 net@6576 net@6315#15nmos@468_poly-left net@6293#3contact@2390_metal-1-polysilicon-1 gnd NMOS L=0.35U W=1.75U AS=1.608P AD=1.914P PS=4.462U PD=3.937U
Mnmos@469 gnd D1#Onmos@469_poly-left net@6303 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=6.931P PS=3.937U PD=17.068U
Mmmos#470 net#6303 net#631542nmos#470 poly-left net#6314 gnd NMOS L=0.350 W=1.750 A5-1.914P AD=1.914P FS=3.9370 DD=3.9370 Mmmos#471 net#6239 net#630441Znmos#471 poly-right and NMOS L=0.350 W=1.750 A5-6.931P AD=1.991P FS=7.7600 DD=5.7750
Mmmos@4/1 hete629/ hete6004#12nmos@4/1 poly=rtght gnd gnd NMMS L=0.350 W=1.750 A=6.591P AU=1.591P E=1.70000 PU=5.750 Mmmos@4/2 net@6318 0822nmos@4/2 poly=left net@6304 qnd NMOS L=0.350 W=1.750 A=6.091P AU=1.591P E=4.4620 PD=3.9370
Mmose4/2 netcosif 200mose4/2 poly-lett nete639 god Meso 1-0.350 w1.150 AS-1.001 AD-1.001 AD-1
Mmmos@474 net@6339 S1#2nmos@474 poly-left net@6349 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=1.914P PS=3.937U PD=3.937U
Mnmos@475 net@6333 net@6340∦12nmos@475_poly-right gnd gnd NMOS L=0.35U W=1.75U AS=6.931P AD=1.991P PS=17.068U PD=5.775U
Mnmos0476 net06349 net06360#2nmos0476_poly-left net06340 gnd NMOS L=0.350 W=1.750 AS=1.608P AD=1.914P PS=4.4620 PD=3.9370
Mmmos@477 gnd D3#3nmos@477 poly-left net@429 gnd NMOS L=0.35U W=1.75U AS=1.914P AD=6.931P PS=3.937U PD=17.068U
Mmmos@478 net66429 S1#6nmos@478 poly-left net66436 qnd NMOS L=0.350 W=1.757 UAS=1.914P AD=1.914P PS=3.9370 PD=3.9370 Mmmos@479 net660444contact@2430 metal-1-n-act net6642042nmos@479 poly-right qnd MMOS L=0.350 W=1.750 AS=6.931P AD=1.991P PS=17.0680 PD=5.7750
<pre>Mmmose4/9 netee404#contacte430 metal=1=n=act netee420#cmmose4/9 poly=right gnd gnd gmds h=0.300 w=1.700 A3=6.931P AD=1.991P F3=1.0660 PD=3.7750 Mmmose4A80 poly=cleft nete6420#cmmose4/9 metal=1-polysilion=1 gnd MMOS L=0.350 W=1.750 A5=1.608P AD=1.914P F5=4.4620 PD=3.9370</pre>
MenergR401 pate (2154) apte at 0141 a pate (141) perceR401 pate and and MMOC T 0 250 M 1 350 MC (0010 DC 13 0000 DD 5 7350
Simulation Time = 272.692 ns Transient Analysis 85.2% done. Simulation Speed: 22.8044 ns/s inter=1 fill-ins: 6412

Figure 29: Generated Spice Deck of Conventional 16-to-1 Multiplexer Layout

9 LTspice XVII - [16-to-1-Mux.spi]	– 0 ×
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▶29日 御休司ののの期間は国務局はお命務通過して中くキシネクジックであられる	
B 16-to-1-Mux.spi = 16-to-1-Mux.spi	
** Extracted Parasitic Capacitors ***	
CO net#6310 0 7.63/FF	
C1 net@6395#3contact@2359 metal-1-polysilicon-1 0 5.15fF	
C2 net#6369 0 19.742FF	
C3 net86297 0 10.126fF	
C4 net@6333#5contact@2373 metal=1-polysilicon=1 0 5.094fF	
C5 nct86404#1contact82374 mctal-1-polysilicon-1 0 7.35fF	
C6 net@6293#3contact@2390 metal=1=polysilicon=1 0 7.135fF	
C7 D0#0contact@2468_metal=1-metal=2 0 7.8221F	
C8 net@6360#3contact@2421 metal=1-polysilicon=1 0 20.552fF	
C9 net@6315#1contact@2403_metal=1=polysilicon=1 0 11.324fF	
C10 net@6304 0 7.359fF	
Cll Dl#3contact@2393_metal-1-polysilicon-1 0 6.04fF	
C12 S0#3contact@2405_metal=1-polysilicon=1 0 4.472fF	
C13 net#6340 0 7.41FF	
C14 D2#3contact02409 metal-1-polysilicon-1 0 4.205fF C15 net06333 0 9.128fF	
C16 S1 0 74.857fr	
C17 net06420#3contact02438 metal=1-polysilicon=1 0 7.408fF	
C10 D3 0 4.606fF	
C19 nct@6404#4contact@2430 metal=1=n=act 0 10.686fF	
C20 S0 0 58.912fF	
C21 net@6315#3contact@2440 metal-1-p-act 0 8.786fF	
C22 D2 0 4.079fF	
C23 D1 0 5.874fF	
C24 D0 0 7.684fF	
C25 net@6609 0 7.637fF	
C26 net@6694#3contact@2477_metal=1-polysilicon=1 0 5.15fF	
C27 net@6668 0 12.038fF	
C28 net06596 0 10.126fF C29 net0663245contact02491 metal=1=polysilicon=1 0 5.094fF	
C30 ncte0632#5contacte2491_mctal-1-polysilcon-1 0 5.094FF C30 ncte6703#1contacte2492_mctal-1-polysilcon-1 0 7.35fF	
C31 neteof03+1contacte2/492 metal=1-polysilicon=1 0 7.33rF C31 neteof592+35contacte2/508 metal=1-polysilicon=1 0 7.135rF	
C32 D4/Contact@2586 metal=1-metal=2 0 7.822F	
C33 net665941contacte2539 metal-1-polysilicon-1 0 20.552fF	
C34 net@6614flcontact@2521 metal-1-polysilicon-1 0 11.324fF	
C35 neL06603 0 7.359FF	
C36 D5#3contact@2511 metal=1=polysilicon=1 0 6.04fF	
C37 S0#21contact02523 metal-1-polysilicon-1 0 4.472fF	
C38 net@6639 0 7.41fF	
C39 D6#3contact@2527_metal=1-polysilicon=1 0 4.205fF	
C40 net@6632 0 9.128FF	
C41 nct@6719#3contact@2556_mctal=1=polysilicon=1 0 7.408fF	
C42 D7 0 4.606fF	
C43 net@6703#4contact@2548 metal-1-n-act 0 10.6861F	
C44 net@6614#3contact@2558_metal=1=p=act 0 8.786fF C45 D6 0 4.079fF	
C45 D5 0 5.874fF	
C40 D3 0 3.8741F	Ÿ

Figure 30: Extracted Parasitic Capacitors Sample of Conventional 16-to-1 Multiplexer Layout

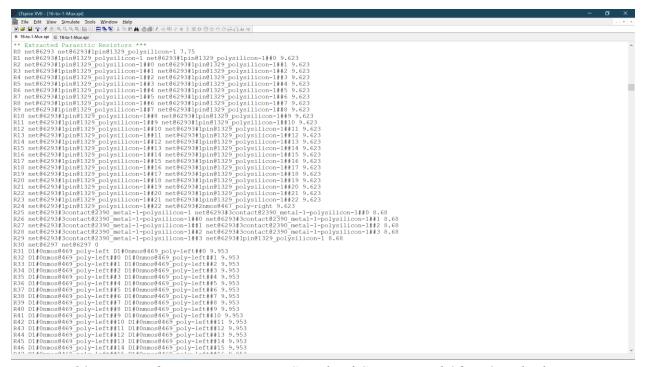


Figure 31: Extracted Parasitic Resistors Sample of Conventional 16-to-1 Multiplexer Layout

بالا المراجع	– ø ×
🚔 File Edit View Simulate Tools Window Help	- 1 X
B 16-to-1-Mux-TG spi	
<pre>P+** SPICE deck for cell 16-to-1-Mux-TG[sch] from library 16-to-1-Mux *** Created on Tue Nov 05, 2019 16:59:31 *** Last rovised on Sat Nov 09, 2019 11:08:26 *** Verliten on Sun Nov 10, 2019 14:18:53 by Electric VLSI Design System, version 9.07 *** Layout tech: mocmos, foundry MOSIS *** UC SFICE ***, MIN_RESIST 4.0, MIN_CAFAC 0.1FF *** UC SFICE ***, MIN_RESIST 4.0, MIN_CAFAC 0.1FF *** SUBCIRCUIT 16-to-1-Mux_4-to-1-Mux-TG FRCM CELL 4-to-1-Mux-TG[sch] .sUBCKT 16-to-1-Mux_4-to-1-Mux_TG B C D S0 S1 Vout *** GLORAL and *** GLORAL and *** GLORAL and *** GLORAL and Munos00 A net0146 net0104 gnd NMOS 1-0.35U W-0.875U Munos02 B S0 net0104 gnd NMOS 1-0.35U W-0.875U Munos02 A so net0146 for 10 Vou f and NMOS 1-0.35U W-0.875U Munos04 D S0 net01468 gnd NMOS 1-0.35U W-0.875U Munos04 D S0 net01468 gnd NMOS 1-0.35U W-0.875U Munos04 D S0 net0146 S0 gnd MMOS 1-0.35U W-0.875U Munos04 D S0 net0146 gnd MMOS 1-0.35U W-0.875U Munos04 D S0 net0145 gnd MMOS 1-0.35U W-0.87</pre>	
Mpmos09 net0104 S0 A vid PMOS L=0.330 W=1.750 Mpmool9 net0104 net0164 B vid PMO Mpmool9 net0104 net0164 B vid PMO Mpmool9 net0104 net0104 Dvid PMO Mpmool9 net0104 net0104 vid PMOS Mpmool9 net0104 vid PMOS L-0.350 W=1.750 Mpmool9 net0104 vid PMOS L-0.350 W=1.750 Mpmool9 net0104 vid PMOS L-0.350 W=1.750 Mpmool9 vid Not L-0.350 W=1.750 Mpmool9 vid S0 net0164 vid Mpmool9 vid S1 net0164 vid Mpmool9 vid S1 net0164 vid vid Mpmool9 vid S1 net0164 vid vid vid Mpmol9 vid S1 net0164 vid vid vid Mpmol9 vid	
.global gnd vdd	
*** TOP LEVEL (ELL: 16-to-1-Mux-TG[ach] X 4-to-1-M80 DO DI D 20 SO SI net89 16-to-1-Mux_4-to-1-Mux-TG X 4-to-1-M81 D4 D5 D6 D7 SO SI net89 16-to-1-Mux_4-to-1-Mux-TG X 4-to-1-M83 D12 D13 D11 SO SI net85 16-to-1-Mux-To-1-Mux-TG X 4-to-1-M83 D12 D13 D14 D15 SO SI net88 16-to-1-Mux 4-to-1-Mux-TG	
A spice Code nodes in cell cell '16-to-1-Mux-TG(sch)' VDD VDD 0 DC 3.3 VDD VDD 0 DC 3.3 VIND VDD 0 DC 0 Vin3 D1 0 PULSE (0 3.3 20n 0.1n 0.1n 10n 320n) Vin3 D1 0 PULSE (0 3.3 20n 0.1n 0.1n 10n 320n) Vin4 D2 0 PULSE (0 3.3 40n 0.1n 0.1n 10n 320n) Vin5 D3 0 PULSE (0 3.3 60n 0.1n 0.1n 10n 320n) Vin5 D3 0 PULSE (0 3.3 80n 0.1n 0.1n 10n 320n) Vin5 D4 0 PULSE (0 3.3 80n 0.1n 0.1n 10n 320n) Vin5 D5 0 PULSE (0 3.3 100n 0.1n 0.1n 10n 320n) Vin5 D5 0 PULSE (0 3.3 100n 0.1n 0.1n 10n 320n) Vin5 D5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 9ULSE (0 3.3 120n 0.1n 0.1n 10n 320n) Vin5 0 PULSE (0 9ULSE (0 9UL	

Figure 32: Generated Spice Deck of Transmission Gate 16-to-1 Multiplexer Schematic

(Tspice XVII - (16-to-1-Mux-TGspi)	– n ×
E File Edit View Simulate Jools Window Help	- 11
■ De Lou Tew Yunname Toop Thuron. Teo S # De W マクシックロットロント	
*** SPICE deck for cell 16-to-1-Mux-TG(lay) from library 16-to-1-Mux *** Created on Thu Nov 07, 2019 16:17:54	~
*** Last revised on Sat Nov 09, 2019 10:47:09	
*** Written on Sun Nov 10, 2019 14:20:31 by Electric VLSI Design System, version 9.07	
*** Layout tech: mocmos, foundry MOSIS	
*** UC SPICE *** , MIN RESIST 4.0, MIN CAPAC 0.1FF	
*** P-Active: areacap=0.9FF/um^2, edgecap=0.0FF/um, res=2.5ohms/sq	
*** N-Active: areacap=0.9FF/um ² 2, edgecap=0.0FF/um, res=3.00hm/sg *** Polytilicop=1 arpacene0.1467EF/um ² 2, edgecap=0.060FF/um, reg=6.20hm/sg	
Torystricon 1. areacap-0.140/11/dm z, eugecap-0.000011/dm, res-0.201ms/sq	
*** Polysilicon-2: areacap=1.0FF/um^2, edgecap=0.0FF/um, res=50.0ohms/sq *** Transistor-Poly: areacap=0.09FF/um^2, edgecap=0.0FF/um, res=2.50hms/sq	
*** Poly-Cut: areacap-0.0FF/um^2, edgecap=0.0FF/um, res=2.20hms/sq	
*** Active-Cut: areacap-0.0FF/um 2, edgecap=0.0FF/um, res=2.50hms/sq	
*** Metal-1: areacap=0.1209FF/um^2, edgecap=0.1104FF/um, res=0.078ohms/sq	
*** Vial: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sg	
*** Metal-2: areacap=0.0843FF/um^2, edgecap=0.0974FF/um, res=0.078ohms/sq	
*** Via2: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.sohms/sq	
Hetai-5, areacap-6,0645ff/um z, eugecap-6,05/4ff/um, res-6,0766fms/3q	
*** Via3: areacap=0.0FF/um ² , edgecap=0.0FF/um, res=0.3ohms/sq	
*** Via4: areacap=0.00F/um2, edgecap=0.0F/um, res=0.80hm3/sq	
*** Metal-5: areacap-0.0843FF/um ² , edgecap=0.0974FF/um, res=0.078ohms/sg	
*** Via5: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=0.8ohms/sq	
*** Metal-6: areacap=0.0423FF/um^2, edgecap=0.1273FF/um, res=0.036ohms/sq	
*** Hi-Res: areacap=0.0FF/um^2, edgecap=0.0FF/um, res=1.0ohms/sq	
*** TOP LEVEL CELL: 16-to-1-Mux-TG(lay)	
Mnmos@40 net@963 net@909#3nmos@40_poly-left D0 gnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mnmos@41 net@963 S0#Onmos@41_poly-left D1 gnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mnmos@42_net@909ilesmos@42_poly-right D2_gnd NMOS_L-0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mmmos43 net6931 S0∲14nmos43 poly-left D3 gnd NMOS L=0.350 №=1.750 AS=1.991P AD=1.991P PS=5.7750 PD=5.7750 Mmmos44 net6962 net6930 net6930 net693 and NMOS L=0.350 №1.750 AS=1.991P AD=1.991P AD=1.991P PS=5.7750 PD=5.7750	
Minioseva netesso netesso signa ando 1-0.500 m-1.750 ks-1.751 ks-1.551 ks-1	
Mnmose46 net@930#4contact@a68 metal-1-metal-2 SI46pin@316 polysilicon-1 gnd gnd MNOS L=0.35U W=1.75U AS=15.772P AD=1.991P PS=43.4U PD=5.775U	
Mnmos@47 net@909#10contact@360 metal-1-n-act S0#8nmos@47 poly-right gnd gnd NMOS L=0.350 W=1.750 AS=15.772P AD=1.991P PS=43.40 PD=5.7750	
Mnmos048 net01144 net01090#3nmos048_poly-left D4 gnd NMOS L=0.350 W=1.750 AS=1.991P AD=1.991P PS=5.7750 PD=5.7750	
Mnmos@49 net@1144 S0#18nmos@49_poly=left D5 gnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mnmos@50 net@1112 net@1090#18nmos@50 poly-right D6 gnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mmmos651 net81112 S0#32nmos651 poly-left D7 qnd NNOS L=0.350 W=1.750 AS=1.991P AD=1.991P AD=5.7750 HD=5.7750 Mmmos652 net81111 net8114 qnd NNOS L=0.350 W=1.750 AS=1.991P AD=1.991P PS=5.7750 HD=5.7750	
Mmmoses2 neteilas neteilas neteila da mos L=0.50 w=1.750 k=1.991r AL=1.991r K=5-3.770 rD=5.7750 rD=5.7750 https://sites.org/alignmoses2 neteilas site/anassis	
Immoses heteliii detiid Strimoses potriete heterii gina anso in color and into and intro and interii terii detiid strimose and interii detiid strimose and interiii detiid	
Mnmos@55 net@100#10contact@426 metal-1-n-act S0#26nmos@55 poly-right gnd MMOS L=0.35U W=1.75U AS=15.772P AD=1.991P PS=43.4U PD=5.775U	
Mnmos@56 net@1273 net@1276#15nmos@56_poly-left D8 gnd NMOS_L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mnmos@57 net@1273 S0#70nmos@57_poly-Teft D9 gnd NMOS L=0.35U W=1.75U AS=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mnmos@58 net@1327 net@13276#12nmos@58 poly-right D10 gnd NMOS L-0.35U W=1.75U AS=1.991P AD=1.991P PA=5.775U PD=5.775U	
Mmmos69 net81327 S0#46mmos69 poly-left D11 and NMOS L=0.35U ₩=1.75U A5=1.991P AD=1.991P PS=5.775U PD=5.775U Mmmos660 net81554 net81271#6mmos60 poly-left net81273 and NMOS L=0.35U ₩=1.75U A5=1.991P AD=1.991P PS=5.775U PD=5.775U	
Mnmos860 net81594 net812/1#onmos860 poly-left net812/3 gnd NMOS L=0.350 W=1.750 AS=1.991P AD=1.991P AS=5.750 PD=5.750 PD=5.750	¥

Figure 33: Generated Spice Deck of Transmission Gate 16-to-1 Multiplexer Layout

9 LTspice XVII - [16-to-1-Mux-TG.spi]	- 0 ×
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▶■■ 予孝しののの思議に回帰る」をも命論は「○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○○	
🖩 1640-1-Mux-TG.spi 🗎 16-10-1-Mux-TG.spi	
** Extracted Parasitic Capacitors ***	^
C0 net@963 0 9.104fF	
C1 D0 0 7.118fF	
C2 D1 0 6.994fF	
C3 net0931_0_8.084fF	
C4 D2 0 7.043±F	
C5 D3 0 7.02fF C6 neL8962 0 11.492[F	
C7 net0930#4contact0360_metal=1=metal=2_0_14.629fF C8_net0909#5contact0366_metal=1=metal=2_0_8.259fF	
Conce909#scontacteson metal-1-metal-2 0 0.2391F Conce8090#10contacte366 metal-1-n-act 0 4.714fF	
C10 S0#4contact@362 metal=1=n=act 0 4.7141F	
Cli S1#8contact@3/2 metal-1-metal-2 0 0.813fF	
C12 note1144 0 9,107FF	
C14 D5 0 6.994fF	
C15 net@1112 0 8.084fF	
C16 D6 0 7.043FF	
C17 D7 0 7.021F	
C10 net@1143 0 17.199fF	
C19 net@1111#4contact@434_metal=1-metal=2 0 14.629fF	
C20 net@1090#5contact@432 metal=1-metal=2 0 8.259fF	
C21 net@1090#10contact@426_metal-1-n-act 0 4.714fF	
C22 S0#22contact0428_metal=1-metal=2 0 16.852fF	
C23 S1#21contact0438 metal-1-metal-2 0 15.152fF	
224 net01273 0 9.104CF	
C25 D8 0 7.118fF C26 D9 0 6.994fF	
(22) http://www.com/arc/arc/arc/arc/arc/arc/arc/arc/arc/arc	
C28 bito 7.043/F	
C29 D11 0 7.02FF	
C30 nct#1594 0 16.809fF	
C31 neL01271 0 14.629[F	
C32 net@1276 0 8.259fF	
C33 net@1276#2contact@492 metal=1=n=act 0 4.714fF	
C34 S0#36contact0494 metaT-1-meta1-2 0 16.819fF	
C35 S1#29contact0504 metal-1-metal-2 0 15.194fF	
C36 net@1414 0 9.104TF	
C37 D12 0 7.118fF	
C38 D13 0 6.994 FF	
C39 net@1382 0 8.084fF	
C40 D14 0 7.043fF	
C41 D15 0 7.02fF C42 neL01413 0 11.492fF	
C42 net@1413 0 11.4921F C43 net@1381#4contact@566 metal=1-metal=2 0 14.6291F	
C43 net#1360#Econtact@564 metal=1-metal=2 0 14.02918 C44 net#1360#Econtact@564 metal=1-metal=2 0 8.259fF	
C45 nete1360#100ntacte558 meta1-1-n-act 0 4.714fF	
C46 S0 011.814fF	
	×

Figure 34: Extracted Parasitic Capacitors Sample of Transmission Gate 16-to-1 Multiplexer Layout

9 LTspice XVII - [16-to-1-Mux-TG.spi]	– a ×
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E 16-to-1-Mux-TG.spi	
** Extracted Parasitic Resistors ***	~
R0 S0#0nmos@41 poly-left S0#0nmos@41 poly-left##0 9.688	
R1 S0#Onmos041 poly-left##0 S0#Onmos041 poly-left##1 9.688	
R2 S0#0nmos041 poly-left##1 S0#0nmos041 poly-left##2 9.688	
R3 S0#Onmos@41 poly-left##2 S0#1pin@333 polysilicon-1 9.688	
R4 net@909 net@909##0 9.858	
R5 net@909##0 net@909##1 9.858	
R6 net@909##1 net@909##2 9.858	
R7 net@909##2 net@909##3 9.858	
R8 net@909##3 net@909##4 9.858	
R9 met#909##4 met#909##5 9.858 R10 met#909##5 met#909##6 9.858	
RID nete909##6 nete909##6 9.858	
R11 nete909##7 nete909##7 9.556	
R13 nete909##0 nete909##0 9.856	
R14 nete909##9 nete909##1 0.9.658	
R15 net8909##10 net8909##11 9.858	
R16 net@909##11 net@909##12 9.858	
R17 net@909##12 net@909##13 9.858	
R18 net@909##13 net@909##14 9.858	
R19 net0909##14 net0909##15 9.858	
R20 net0909##15 net0909##16 9.858	
R21 net0909##16 net0909##17 9.858	
R22 net@909##17 net@909##18 9.858	
R23 net@909##18 net@909##19 9.858	
R24 net@909##19 net@909##20 9.858	
R25 net@909##20 net@809##21 9.858	
R26 net@909##21 net@909##22 9.658	
R27 net8909##22 net8909##23 9.858 R28 net8909##23 net8909#i2ine2809#i2ine330 polysilicon-1 9.858	
rz∂ nete909≢#z.s nete909≢fDine320_porysilicon-1 9.858 R29 nete909≢2pmose41 poly-left nete909#2pmose41 poly-left≢#0 9.688	
RZS HELESUS#ZEJMUSE41_DOIY-LEIL HELESUS#ZEJMUSE41_DOIY-LEIL##0 5.000 RZS HELESUS#ZEJMUSE41_DOIY-LEIT##10 HELESUS#ZEJMUSE41_DOIY-LEIL##1 9.688	
R31 nete959#2pmos@d1 poly-left##1 nete909#2pmos@d1 poly-left##2 9.688	
N31 nete90942pm0841 poly-left##1 nete909 9.688	
R33 net@909#3nmos@40 poly-left net@909#3nmos@40 poly-left##0 9.688	
R34 net@909#3nmos@40 polv-left##0 net@909#3nmos@40 polv-left##1 9.688	
R35 net@909#3nmos@40 polv-left##1 net@909#3nmos@40 polv-left##2 9.688	
R36 net@909#3nmos@40 poly-left##2 net@909#4pin@335 polysilicon-1 9.688	
R37 net@909 met@909##0 9.743	
R38 net0909##0 net0909##1 9.743	
R39 net0909##1 net0909##2 9.743	
R40 net@909##2 net@909##3 9.743	
R41 net@909##3 net@909##4 9.743	
R42 net@909##4 net@909##5 9.743	
R43 net@909##5 net@909#4pin@335_polysilicon-1 9.743	
R44 net@909#5contact@366 metal-1-metal-2 net@909#5contact@366 metal-1-metal-2##0 9.3	
R45 net8909#55contact@366 metal-1-metal-2##0 net8909#5contact@366 metal-1-metal-2##1 9.3	
R46 net0909#5contact0366 metal-1-metal-2##1 net0909#5contact0366 metal-1-metal-2##2 9.3	

Figure 35: Extracted Parasitic Resistors Sample of Transmission Gate 16-to-1 Multiplexer

Layout

Section 7: LTSPICE Simulations:

After creating the schematic and layout design of the 16-to-1 Multiplexer, waveforms were created using LTSPICE. Theses waveforms were created by using Spice Code (Figure 27) to initialize our VDD, GND, and our many inputs, D0-D15, and S0-S3, so that it could test certain computations. The computations that we tested set each input (D0-D15) for 50 nanoseconds at different times, then back to low; in other words, 100 nanoseconds period, with rise time and fall time of 5 nanoseconds and 50% duty cycle. Each of the inputs were high at different times so they wouldn't be able to relate to each other. After that, we set tested all the computations for the selector (S0-S3), starting from 0 to 15. This way, it'll be able to output each individual input and show a wavelike output. The computations that it tested are the same between the schematic and layout. We were able to verify the waveforms obtained from LTSPICE were correct by matching it with the truth table on Table 1.

Section 7.1: Schematic:

For the schematic, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the inputs and confirming that the output shows a wavelike form.

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Lispice XVII - [16-to-1-Muxspi] Ele View Plot Settings Simulatio Plat G Spick A & G & K Pris 1 16 po Antar Spice - 1-Mux p)	n Iools Wind	dow <u>H</u> elp Mana ana ana ana ana ana ana ana ana ana	1 冬 卓 子 文 ひ 徳	୧୯ ୩ ୯ଲିଲିକ	AP.									- 6 ×
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1.74-10	Ŭ	0	0	0	0	0	0	0	0	0	0	0	0	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1.7v- 0 1	~	0	0	0	0	0	0	0	0	0	0	0	0	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		1	0	0	0	0	0	0	0	0	0	0	0	0	0
1.74 0		0	1	0	0	0	0	0	0	0	0	0	0	0	0
1.7v-000000000000000000000000000000000000	1.7V- 0 0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	1	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	1	0	0	0	0	0	0	0	0	0
	1.7V OO	<u> </u>	<u> </u>		<u> </u>		1	0	0		0	0	0	0	О

Figure 36.1: LTSPICE Waveforms of Schematic Design of a 16-to-1 Multiplexer (Inputs)

Lispice XVII - [16-to-1-Muxs Elle View Plot Settings	Simulation Tools V	Mindow <u>H</u> elp anci na ⊟ /→	→田く中 3 本ひぐ	୬ଅ ୩ ୯ଲିଲି	de ap		V(d8)							- 0 ×
1.7V- 0 0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
^{1.7v} 0 0		0	0	0	0	0	0	1	0	0	0	0	0	0
		0	0	0	0	0	/(d10) 0	0	1	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	0	0	0	0
		0	0	0	0	0	0	0	0	0	1	0	0	0
1.7V- 0 0		0	0	0	0	0	0	0	0	0	0	1	0	0
1.7V-000	014	0	0	0	0	0	^{/(d14)}	0	0	0	0	0	1	0
^{1.7v} 0 0	0	0	0	0	0	0	^{/(d15)}	0	0	0	0	0	0	1
0.0V- 0.0µs	0.2µs		0.4µs		0.6µs		0.8µs		1.0µs		1.2µs	,	1.4µs	1.6µs

Figure 36.2: LTSPICE Waveforms of Schematic Design of a 16-to-1 Multiplexer (Inputs)



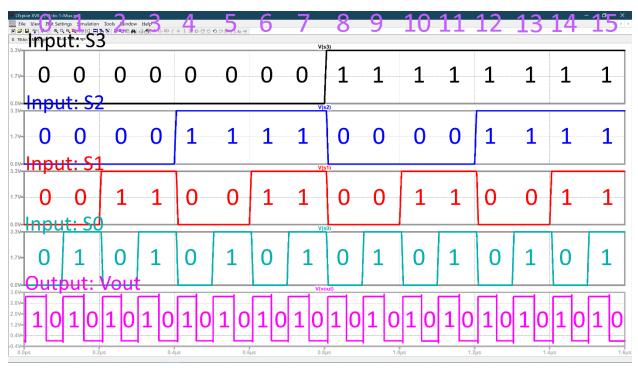


Figure 37: LTSPICE Waveforms of Schematic Design of a Conventional 16-to-1 Multiplexer (Outputs)

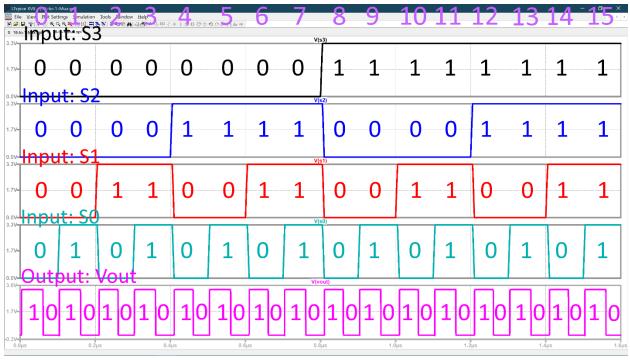


Figure 38: LTSPICE Waveforms of Schematic Design of a Transmission Gate 16-to-1 Multiplexer (Outputs)

Section 7.2: Layout:

For the layout, we tested both conventional 16-to-1 Multiplexer, and Transmission Gates 16-to-1 Multiplexer. We could confirm that it works by viewing the inputs and confirming that the output shows a wavelike form.

10.0	16-to-1-Mux-TG.spi] Plot Settings Simulat	ion Iools Wir 마이 사용	dow Help 하려고 하루는 영	D <> ÷ 3 文1D 신	900684	t ap		V(d0)							- 0 ×
3.3V 1.7V-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1.7V - O	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1.7V- 0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1.7V-	0		1	0	0	0	0	0	0	0	0	0	0	0	0
			0	1	0	0	0	0	0	0	0	0	0	0	0
3.3V 1.7V- O		0	0	0	1	0	0	0	0	0	0	0	0	0	0
3.3V- 1.7V- 0.0V-		0 _0	0	0	0	1	0	V(d6)	0	0	0	0	0	0	0
1.7V-0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0.0V- 0.0µs	().2µs	(0.4µs		0.6µs		0.8µs		1.0µs		1.2µs		1.4µs	1.6µ

Figure 39.1: LTSPICE Waveforms of Layout Design of a 16-to-1 Multiplexer (Inputs)

LTspice XVII - [16 Eile View Plo		on Tools Wir	dow Help												- 0 ×
1nn	ut:D8	833 X 201	8 8 2 8 2 4 4)くキ } 空むぐ	90 0 066	ta sp									
3.3V	-	, 	•	•	•	•	•	V(d8)	•	•	•	•	•	•	•
1.7٧	0	0	0	0	0	0	-0-	11	0	0	0	0	0	0	0
^{0.0V}	ut:D)						V(d9)							
1.7V-	0_	Q	0	0	0	0	0	0	1	0	0	0	0	0	0
0.0V np	ut:D	10					<u> </u>	(d10)							
1.7V	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
3.3V							N	/(d11)							
1.7V		ρ	0	0	0	0	0	0	0	0	1	0	0	0	0
3.3V	ut.D.	. 2					<u>`</u>	((d12)							
1.7V O		_Q	0	0	0	0	0	0	0	0	0	1	0	0	0
3.3V	0		0	0		0	0	((d13)		0		0		0	0
1.7V- O	U ut·D1	4	0	0	0	0	0	0	0	0	0	0	11	0	0
3.3V		. <u> </u>	0	0	0	0	-	((d14)	0	0	0	0	0	11	0
1.7V-		U	0	0	U	U	0	U	U	0	0	0	0		0
3.3V		5	~	~	~	•	~	(d15)	~	_	~	~	~		
1.71	U	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.0V= 0.0µs	0	.2µs).4µs		0.6µs		0.8µs		1.0µs		1.2µs		1.4µs	1.6µs

Figure 39.2: LTSPICE Waveforms of Layout Design of a 16-to-1 Multiplexer (Inputs)



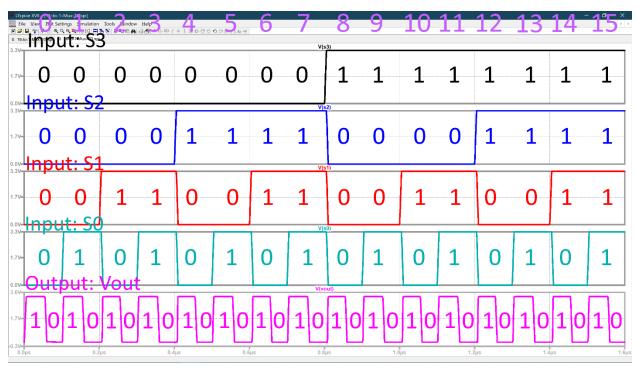


Figure 40: LTSPICE Waveforms of Layout Design of a Conventional 16-to-1 Multiplexer (Outputs)

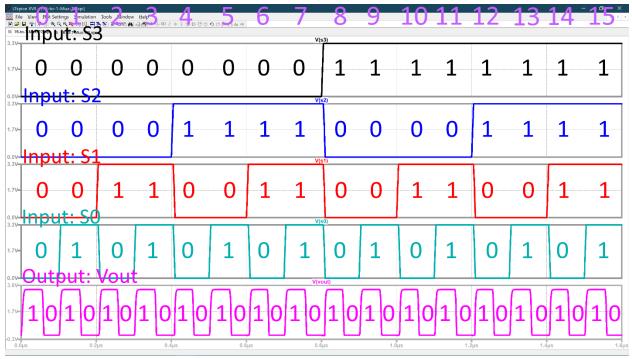


Figure 41: LTSPICE Waveforms of Layout Design of a Transmission Gate 16-to-1 Multiplexer (Outputs)

Section 7.3: Comparison:

For LTSPICE, by comparing Figure 37 (Conventional Schematic), Figure 38 (Transmission Gate Schematic), Figure 40 (Conventional Layout), and Figure 41 (Transmission Gate Layout) with each other, the way the output reacted given the certain inputs appears to be the same. In addition, with the inputs we gave, it gave us the appropriate outputs that we were looking for, so it confirms that our design is correct. The outputs that we were looking from could be seen by using the truth table on Table 1. The only noticeable difference between the figures would be the propagation delay and the way the waveforms looked, which could be seen on Table 6. For Figure 37, the output almost looks like a perfect square waveform, with similar rise and fall times; it has some parts where it peaks up. For Figure 38, the output waveform appears to have a longer fall time but appear as almost like a perfect square waveform. For Figure 40, the output waveform appears to have a longer rise time and fall time, but still appear as a square waveform (a bit curvier). For Figure 41, the output waveform appears to have a really long rise time and fall time, but still appears as a square waveform (a lot more curvier); this is probably because of the long rise time and fall time, which causes it to not stay high for very long before it has to go back to low. Depending on the which design, each has its own different propagation delay.

In conclusion, LTSPICE shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time, and propagation delay. The differences can be viewed on Table 6, which has a summary of the measurements.

Section 8: Measurement Summary:

The rise time, fall time, and propagation delay of gates of entire I/O are all shown on the table below, Table 6. It's found that for LTSPICE, the Schematic is faster compared to the Layout; the delay times are less, and it's rise and fall time are shorter. It's also found that for the IRSIM, the Schematic is faster compared to the Layout; the delay times are less. Furthermore, Table 7 provides more measurements for each of the designs, such as the transistor sizes, power dissipation, and total chip area. It's found that the transmission gate takes a lot less power and area compared to the conventional CMOS. This is because it uses less transistors compared to the conventional resulting in less power to power the transistors.

	Rise Time	Fall Time	Propagation Delay
Conventional LTSPICE Schematic	103.54 ns - 103.42 ns = 0.12 ns	158.92 ns - 158.72 ns = 0.20 ns	$T_{HL} = 1 \text{ ns},$ $T_{LH} = 0.90 \text{ ns}$
Conventional LTSPICE Layout	104.70 ns - 104.20 ns= 0.50 ns	161.37 ns - 160.65 ns = 0.72 ns	$T_{HL} = 1.4 \text{ ns}$ $T_{LH} = 1.5 \text{ ns}$
Conventional IRSIM Schematic	N/A	N/A	Between 0.70ns - 1.55 ns
Conventional IRSIM Layout	N/A	N/A	Between 0.85 ns- 1.60 ns
Transmission Gate LTSPICE Schematic	105.20 ns - 101.20 ns = 4.00 ns	160.00 ns - 150.00 ns = 1.00 ns	$T_{HL} = 0.18 \text{ ns}$ $T_{LH} = 0.20 \text{ ns}$
Transmission Gate LTSPICE Layout	110.00 ns - 101.00 ns = 9.00 ns	160.90 ns - 155.20 ns = 5.70 ns	$T_{HL} = 0.82 \text{ ns}$ $T_{LH} = 0.85 \text{ ns}$
Transmission Gate IRSIM Schematic	N/A	N/A	Between 0.50 ns - 1.20 ns
Transmission Gate IRSIM Layout	N/A	N/A	Between 0.70 ns- 1.45 ns

Table 6: Summary of Measurements

	Conventional	Conventional	Transmission	Transmission
	Schematic	Layout	Gate Schematic	Gate Layout
Transistor Sizes	PMOS (10/2),	PMOS (10/2),	PMOS (10/2),	PMOS (10/2),
(W/L)	NMOS (5/2)	NMOS (10/2)	NMOS (5/2)	NMOS (10/2)
Transistor Counts	Inverter = 2	3-AND = 8	4-to-1 = 16	4-to-1 = 16
	AND = 6	4 - OR = 10	16-to-1 = (16*5)	16-to-1 = (16*5)
	3-AND = 6 + 6 =	Inverter = 2	= 80	= 80
	12	4-to-1 = (8*4) +	Total = 80	Total = 80
	OR = 6	10 + (2*2) = 46		
	4 - OR = 6 + 6 + 6	16-to-1 = (46*5)		
	= 18	= 230		
	4-to-1 = (4*12) +	Total = 230		
	18 + (2*2) = 70			
	16-to-1 = (70*5) =			
	350			
	Total = 350			
Total Chip Area	Х	17126.1891 um ²	Х	12288.4727 um ²
Power Dissipation	3.3 V * 0.0032 A	3.3 V * 0.0044 A	3.3 V * 0.0023 A	3.3 V * 0.0029 A
	= 0.01056 Watts	= 0.01452 Watts	= 0.00759 Watts	= 0.00957 Watts

 Table 7: More Measurements

<u>Calculations:</u>

Conventional: Size = $1077.5 \lambda x 519 \lambda = 188562.5 \text{ nm} x 90825 \text{ nm} = 17126.1891 \mu m^2$

Transmission Gate: Size = $387.5 \lambda x 1035.5 \lambda = 67812.5 \text{ nm } x 181212.5 \text{ nm} =$

 $12288.4727 \ \mu m^2$

Section 9: Conclusion:

In this project, we designed a CMOS of a 16-to-1 Multiplexer by connecting five 4-to-1 Multiplexers together. A conventional 4-to-1 Multiplexer is designed by connecting 4 three input AND gates, 1 four input OR gate, and two inverters together. A transmission gate 4-to-1 Multiplexer is designed by connecting six transmission gates, and two inverters together. By using the Electric software, we created four different designs, a conventional schematic design, a conventional layout design, a transmission gate (TG) schematic design, and a transmission gate (TG) layout design. We also generated waveforms using two different software, IRSIM and LTSPICE. The two different software helped support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the four different design, we compared them and observe their similarities and differences. We observed that for LTSPICE and IRSIM, the input and output reacted the same way given certain inputs for both the Electric Schematic and for the Electric Layout; in addition, it matched the computed values and the goal we were trying to achieve. The only difference between the Electric Schematic and the Electric Layout were the rise time, fall time, and propagation delay. For LTSPICE and IRSIM, these forms of differences can be observed by checking out Table 6, Summary of Measurements. Another thing that we compared were the differences between conventional CMOS and transmission gates. Based off Table 7, it's found that transmission gates take less area and power compared to the conventional CMOS. This is because transmission gates are used to help simplify circuitry and because there's less transistors, there's less power needed to run all those transistors. Therefore, based on our observation and the data that was gathered, we can conclude that there isn't a significant difference in terms of the waveforms; however, there is a difference in the rise time, fall time and propagation delay when zooming in on the waveform. In addition, using transmission gates are more efficient compared to using regular convention CMOS because it saves on the amount of transistors, space, and power.

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