

EE457: Digital IC Design <u>Fall Semester 2019</u> Project #2 Report Cover Sheet Due 10/21/2019

*PROJECT TITLE: <u>16-Bit Ripple Carry Adder</u>

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Sections	GRADE Points
1. Executive Summary	/5
2. Introduction	/5
3. Electric Circuit Schematic	/10
4. LTSpice simulations of Schematic (label waveforms)	/10
5. IRSIM simulations of Schematic (label waveforms)	/10
6. Electric Layout	/25
7. LTSpice simulation of Layout	/10
8. IRSIM Simulations of Layout	/10
9. Summary of Measurements in	
a) Propagation delays of gates and entire I/O,	/3
b) Total Chip area in um ²	/2
10. Comparisons of Schematic & Layout	/5
11. Conclusion	/5
TOTAL	/100

*Do not hand-write.

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Section 1: Executive Summary:

In this project, we will be designing a CMOS of a 16-Bit Ripple Carry Adder using Electric. By using the Electric software, we'll be creating two different designs, a schematic design and a layout design. In order to test if our designs are correct, we'll be generating waveforms to test for correctness by giving a specific input and expecting a certain output. We'll be generating the waveforms using two different software, IRSIM and LTSPICE. The two different software would help support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we'll compare them and observe their similarities and differences.

To design a 16-Bit Ripple Carry Adder, we plan to use two different designs and combining them together to make a Full Adder. One design we plan to use is a two input XOR gate and the second design we plan to use is a two input NAND gate. By combining two XOR gates and three NAND gates, we'll be able to obtain a Full Adder. After making the Full Adder, we create 15 more Full Adders and link them together to create a 16-Bit Ripple Carry Adder. We would also test each individual design using waveforms before putting them together to make sure they satisfy our requirements. By testing each individual design would also help with the debugging process when combining the two designs together because we'll know where the problem lies in case the waveform doesn't turn out like the way expected. Section 2: Background and Approach:

A 16-Bit Ripple Carry Adder is a form of digital circuit that is used to produce the arithmetic sum of two binary number. It could also be seen in terms of an arithmetic expression, such as F = A + B. The 16-Bit Ripple Carry Adder would add each bit at a time, starting from the least significant bit to the most significant bit. It adds each bit by utilizing the Full Adder that's already implemented in the 16-Bit Ripple Carry Adder.

The approach we plan to take to design the 16-bit Ripple Carry Adder would be to use two different designs and combining them together. The two designs that we plan to use would be a two input XOR gate and two input NAND gate. The reason for this approach is because we can't directly build a CMOS 16-Bit Ripple Carry Adder without first building a Full Adder, and we can't build a Full Adder without using a two input XOR gate and two input NAND gates. By applying two XOR gates and three NAND gates, we'll be able to obtain a Full Adder. After making the Full Adder, we create 15 more Full Adders and link them together to create a 16-Bit Ripple Carry Adder. The figures on the next few pages show the schematic and layout of the two input XOR gate is shown on Table 1; the truth table of a two input NAND gate is shown on Table 2; the truth table of a Full Adder is shown on Table 3.

Input: A	Input: B	Output: A XOR B
0	0	0
0	1	1
1	0	1
1	1	0





Figure 1: Schematic Design of a Two Input XOR Gate



Figure 2: Layout Design of a Two Input XOR Gate (Landscape)

Input: A	Input: B	Output: A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Table 2: Truth Table of a Two Input NAND Gate



Figure 3: Schematic Design of a Two Input NAND Gate



Figure 4: Layout Design of a Two Input NAND Gate (Portrait)

Input: Carry	Input: A	Input: B	Output: Sum	Output: Carry
In				Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 3: Truth Table of a Full Adder



Figure 5: Schematic Design of a Full Adder



Figure 6.0: Layout Design of a Full Adder Overview (Landscape)



Figure 6.1: Layout Design of a Full Adder Zoomed Left Side (Landscape)



Figure 6.2: Layout Design of a Full Adder Zoomed Middle Side (Landscape)



Figure 6.3: Layout Design of a Full Adder Zoomed Right Side (Landscape)

Section 3: Electric Schematic:

We created a schematic of the 16-Bit Ripple Carry Adder by combining 16 Full Adders (Figure 5) together, using its icon. It was combined by connecting the Cout of the Full Adder to the Cin of the next Full Adder. Figure 7 shows the schematic design that was built using Electric of the 16-Bit Ripple Carry Adder. Figure 8 shows the Design Rule Check (DRC) that was performed on the schematic; it indicates that there were no errors or warning with the schematic.



Figure 7: Schematic Design of a 16-Bit Ripple Carry Adder

😟 Electric Messages	
	======24===============================
Checking schematic cell	'NAND{sch}'
No errors found	
Checking schematic cell	'XOR{sch}'
No errors found	
Checking schematic cell	'FullAdder{sch}'
No errors found	
Checking schematic cell	'16-Bit-Adder{sch}'
No errors found	
0 errors and 0 warnings	found (took 0.063 secs)

Figure 8: Design Rule Check (DRC) of a 16-Bit Ripple Carry Adder Schematic Design

Section 4: LTSPICE for Electric Schematic:

After creating the schematic design of the 16-Bit Ripple Carry Adder, waveforms were created using LTSPICE. The waveforms were created by using Spice Code to initialize our VDD, GND, and our 33 inputs, A (0-15), B (0-15), and Cin. It was also used to produce the type of analysis we want; in this case, we used a transient analysis, which goes as far as 80ns.

The Spice Code that we wrote is shown on Figure 9. It provides certain values to the inputs so that it'll be able to perform the following computations, 107 + (-32) = 75, 16 + (-28) = -12, 52378 + 589 = 52967, and -71 + (-10000) = -10071. In addition, Table 4 shows the inputs in binary and the outputs that was obtained from both computation and LTSPICE.

Vin Cin 0 DC 0
Vin2 A0 0 PULSE (3.3 0 20n 0.01n 0.01n 40n 80n)
Vin3 A1 0 PULSE (3.3 0 20n 0.01n 0.01n 20n 40n) Vin4 A2 0 DC 0
Vin5 A3 0 PULSE (3.3 0 20n 0.01n 0.01n 20n 60n)
Vin6 A4 0 PULSE (3.3 0 0 0.01n 0.01n 20n 80n)
Vin7 AS 0 PULSE (3.3.0 20n 0.01n 0.01n 40n 80n)
Ving A7 0 PULSE (3.3 0 0 0.01n 0.01n 40n 80n)
Vin10 A8 0 PULSE (3.3 0 0 0.01n 0.01n 60n 80n)
Vin11 A9 0 PULSE (3.3 0 0 0.01n 0.01n 60n 80n)
Vin12 A10 0 PULSE (3.3 0 0 0.01n 0.01n 40n 80n)
Vint3 A110 POLSE (3.3 0 0 0.011 0.011 401 801)
Vin15 A13 0 PULSE (3.3 0 0 0.01n 0.01n 60n 80n)
Vin16 A14 0 PULSE (3.3 0 0 0.01n 0.01n 40n 80n)
Vin17 A15 0 PULSE (3.3 0 0 0.01n 0.01n 40n 80n)
Vin18 B0 0 PULSE (3.3 0 0 0.01n 0.01n 40n 60n)
Vin 20 B2 0 PULSE (3 3 0 0 0 0 1 n 0 0 1 n 20 n 60 n)
Vin21 B3 0 PULSE (3.3 0 0 0.01n 0.01n 40n 60n)
Vin22 B4 0 PULSE (3.3 0 0 0.01n 0.01n 60n 80n)
Vin23 B5 0 PULSE (3.3 0 40n 0.01n 0.01n 20n 40n)
Vin25 B7 0 PULSE (3.3 0 40n 0.01n 0.01n 20n 40n)
Vin26 B8 0 PULSE (3.3 0 40n 0.01n 0.01n 40n 40n)
Vin27 B9 0 PULSE (3.3 0 60n 0.01n 0.01n 20n 20n)
Vin28 B10 0 PULSE (3.3 0 40n 0.01n 0.01n 40n 40n)
Vin29 B110 P0LSE (3.3.0 40n 0.01n 0.01n 20n 40n)
Vin31 B130 PULSE (3.3 0 40n 0.01n 0.01n 40n 40n)
Vin32 B14 0 PULSE (3.3 0 40n 0.01n 0.01n 20n 40n)
Vin33 B15 0 PULSE (3.3 0 40n 0.01n 0.01n 20n 40n)
include C:\Users\kille\Desktop\Electric\C5_models.txt

Figure 9: Spice Code Written for LTSPICE

	First Computation	Second Computation	Third Computation	Fourth Computation
Input: A	107	16	52378	-71
	(0000000001101011)	(0000000000010000)	(1100110010011010)	(1111111110111001)
Input: B	-32	-28	589	-10000
	(1111111111100000)	(1111111111100100)	(0000001001001101)	(1101100011110000)
Output:	75	-12	52967	-10071
Expected	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)
Sum				
Output:	75	-12	52967	-10071
LTSPICE	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)
Sum				

Table 4:	Inputs and	1 Outputs	of the	Computations	(Schematic)
1 4010 11	inputs and	· Outputs	or the	compatitions	(Demennance)

UTspice XVII - (16-Bit-Adder.spi) Eile View Plot Settings Simulation P의민국가 관육 속 수 속 비용는 목록 1, 3 위 ≥ 16-Bit-Adder.spi = 16-Bit-Action.sp	Iools Alindow Help ຂ⊛∦∦∄≮ ⊹ຫ≳≑3ຮ⊳ອະອດຣິດໂ	6 V(a15)	5237	/8 -71	- 01 X
^{3.3V} 1.7V-Input: A15 0		0	1	1	
^{3.3V} ^{1.7V-} Input: A14 0		0	1	1	
^{3.3V} ^{1.7V} Input: A13 (0	0	1	
^{3.3V} ^{1.7V} Input: A12 0		0	0	1	
^{3.3V} ^{1.7V} Input: A11 0			1	1	
^{3.3V} ^{1.7V} Input: A10 0		0	1	1	
^{3.3V} ^{1.7V} Input: A9 0		0	0	1	
^{3.3V} ^{1.7V-} Input: A8 0		0	0	1	
^{3.3V} ^{1.7V} Input: A7 0		V(a7)	1	1	
Ons 8ns	16ns 24ns	32ns 40ns	48ns 5	ns 64ns 72ns	80ns

Figure 10.1: LTSPICE Waveforms of Schematic Design of 16-Bit Ripple Carry Adder (A15-A7)

ダ LTspice XVII - [16-Bit-Adder.spi] Elle View Plot Settings Simulation Iools Window He アメリアンズ していたい アンチョン (1995)	elp J x p-20 c c c c a a m		- Ø	× 2 x
▶ 16-Bit-Adder.spi				
^{3.3V-} 1.7V- Input: A6 1	0		0	
^{3.3V} 1.7V- Input: A5 1	0		1	
^{3.3V} 1.7V-Input: A4 0	1		1	
^{3.3V} 1.7V- 0.0V	0		1	
^{1.0mV} Input: A2 0.0mV 0	0		0	
^{3.3V} 1.7V-Input: A1 1	0		0	
^{3.3V} 1.7V Input: A0 <u>1</u>	0	0	1	
1.0mV 1 pout: Cip -		V(cin)		
-1.0mV- 0ns 8ns 16ns	0 24ns 32ns	40ns 48ns	66ns 64ns 72ns	80ns

Figure 10.2: LTSPICE Waveforms of Schematic Design of 16-Bit Ripple Carry Adder (A6-A0)

✓ LTspice XVII - [16-Bit-Adder.spil Eile View Plot Settings Sin lation ▶ # 대 귀 소 이 속 속 List · · · · · · · · · · · · · · · · · · ·	pols Window Help ▲ 상류 / 는 면 २ 후 3 文 2 2 2 2 2 2 1 4	y(b15)	589	-1000°
^{3.3v-} Input: B15 <u>1</u>	1	V(b14)	0	1
^{3.3V} ^{1.7V-} Input: B14 <u>1</u>	1	V(513)	0	1
^{3.3V} ^{1.7V} Input: B13 <u>1</u>	1	V(b13)	0	0
^{3.3V} ^{1.7V} Input: B12 1	1	V(012)	0	1
^{3.3V} ^{1.7V} Input: B11 <u>1</u>	1	V(011)	0	1
^{3.3V} 1.7V-Input: B10 1	1		0	0
^{3.3V} ^{1.7V} Input: B9 <u>1</u>	1	V(b9)	1	0
^{3.3V} ^{1.7V-} Input: B8 <u>1</u>	1	V(b8)	0	0
^{3.3V} ^{1.7V} Input: B7 1	1	V(b7)	0	1
Ons 8ns	16ns 24ns	32ns 40ns	48ns 56ns	s 64ns 72ns 80ns

Figure 10.3: LTSPICE Waveforms of Schematic Design of 16-Bit Ripple Carry Adder (B15-B7)

1put: B6 🧃	4	V(D6)	
<u> </u>	1	L L	
		/(b5)	
iput: B5 <u>1</u>		0	1
		/(b4)	4
iput: B4 U	U	U	
		/(b3)	
nput: B3 U	U		0
	1	1	0
ipul. dz U			U
nput: B1 👝	0		0
0	0	((b0)	0
	Δ	1	\cap
	U	_	U

Figure 10.4: LTSPICE Waveforms of Schematic Design of 16-Bit Ripple Carry Adder (B6-B0)

UTspice XVII - [16-Bit-Adder.sp. Elle View Plot Settings Simulation Trajs Window Part 가게 속 및 및 및 및 문화 및 및 문화 및 가귀 / 는 파구	Help ≑3호₽೮৫ 5€@0, #	5296	57 -1(0071
Output: Sum 15		V(sum15)		
1.6V-	_ [1	1	*	1
0.4V Output: Sum 14		V(sum14)		–
3.6V- 1.6V-	1	1		1
^{0.4V} Output: Sum 13		V(sum13)		
1.6V -	1	0		0
3.6V Output: Sum 12		V(sum12)		
1.6V -	1	0		1
^{0.4V} Output: Sum 11		V(sum11)		
1.6V-	1	1		1
3.6v Output: Sum 10		V(sum10)		
1.6V-] 1	1		0
3.6V Output: Sum 9		V(sum9)		
1.6V- 0	∫ 1			
3.6V Output: Sum 8		V(sum8)		
1.6V -	1	0		0
3.6V Output: Sum7		V(sum7)		
1.6V-	1	1		1
-0.4V Ons 8ns 16ns	24ns 32ns	40ns 48ns	56ns 64ns	72ns 80ns

Figure 10.5: LTSPICE Waveforms of Schematic Design of 16-Bit Ripple Carry Adder (Sum15-Sum7)



Figure 10.6: LTSPICE Waveforms of Schematic Design of 16-Bit Ripple Carry Adder (Sum6-

Sum0)

Section 5: IRSIM for Electric Schematic:

After creating the schematic design of the 16-Bit Ripple Carry Adder, waveforms were created using IRSIM. Theses waveforms were created by configuring the inputs, A and B, so it could test certain computations. The computations we tested are the same as what's shown in Table 4 (same values as the LTSPICE), also shown on Table 5. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify that the waveforms obtained from IRSIM matches on Table 5.

Figure 11, 12, 13, and 14 shows the IRSIM waveforms for the 16-Bit Ripple Carry Adder.

	First Computation	Second Computation	Third Computation	Fourth Computation
Input: A	107	16	52378	-71
	(000000001101011)	(000000000010000)	(1100110010011010)	(1111111110111001)
Input: B	-32	-28	589	-10000
	(1111111111100000)	(1111111111100100)	(0000001001001101)	(1101100011110000)
Output:	75	-12	52967	-10071
Expected	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)
Sum				
Output:	75	-12	52967	-10071
IRSIM Sum	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)

Table 5: Inputs and Outputs of the Computations (Schematic)

🙂 Electric			- 🗆 ×
File Edit Cell Export Vi	iew Window Tools Help	107 + (-32) = 75	
i 🙆 🗟 📐 🖑 🔾 🦾	ء 💭 🗮 📑 🖪 💦 🎉 💁 🗢 🗉	107 (32) = 73	
Simulation of Tipple any Components		111111111111100000 = 000	
Explorer Layers	⊞₽ к∢∎⊁н≜▼	Time Os 0.5ns 1ns 1.5ns	2ns 2.5ns 3ns 3.5n
FullAdde@73	¹ Input: A15 ^{× •}		0
	² A14 Input: A14 × • × ×	-	0
FullAdde@80	^³ Input: A13 ^{× □ ※}		0
€ FullAdde@84 FullAdde@85 FullAdde@86	⁴ Input: A12 ^{× •} ×		0
FullAdde@87	⁵ Input: A11 ^{× •}		0
• A1 • A2 • A3	¹⁰ Input: A10 ^{× •} × ×		0
	⁷ Input: A9 × • × • × ×		0
• A8 • A9 • A10	ÅInput: A8 × • × • × •		0
• A11 • A12 • A13 • A14	^Å Input: A7 × • × • × •		0
- + A15 - + B0			v
NOTHING SELECTED SIZ	E: 184.5 x 125.5 TECH: schematic		(-53, 112)

Figure 11.1: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)



Figure 11.2: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (107 + (- 32) = 75)

😃 Electric		– 🗆 X
<u>File Edit C</u> ell E <u>x</u> port <u>V</u> i	iew Window Iools Help $107 + (-32) = 75$	
🔁 🗟 📐 🖑 📿 –	● ♯ 0.5 ┆┆ 👎 🖪 🐚 饕 🕿 🔛 🗧 ⇒ 🔿 🛥 🛨 🛛 📍 🕇 💙 🖓 💭 👘 🌔 💆	
Simulation of Tople carry Components	10001101011 + 1111111111111100000 = 00	
Explorer Layers	Image:	2ns 2.5ns 3ns 3.5n
FullAdde@73	¹⁸ Input: B15 ^{× □ ★ XX}	1
FullAdde@76 FullAdde@78 FullAdde@79 FullAdde@79	¹⁹ Input: B14 ^{× □ X X}	1
FullAdde@81	²⁰ Input: B13 ^{× □ × ≭}	1
€ FullAdde@84 FullAdde@85 FullAdde@86 FullAdde@86 FullAdde@87	²¹ Input: B12 ^{× □ ★ ★}	1
FullAdde@88 FullAdde@89 A0	²² B11Input: B11 ^{× • × **}	1
• A1 • A2 • A3	23 B10 Input: B10 ^{× □ × ∞}	1
	²⁴ Input: B9 × □ × ℤ	1
A8 A9 A10	²⁵ Input: B8 × □ ¥ ₩	1
A11 A12 A13 A14	²⁶ ^{B7} Input: B7 × □ × ℤ	1
		(52 112)
NOTAINO SELECTED SIZI	L. 10% J A 123.J TECH, Schematic	(-53, 112)

Figure 11.3: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)



Figure 11.4: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (107 + (- 32) = 75)

🤨 Electric	– 🗆 X
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u> iew <u>W</u> indow <u>T</u> ools <u>H</u> elp	107 + (-32) = 75
🚵 🗄 📐 🖑 Q. 🖸 🔎 🗰 0.5 🗮 👎 🖪 🐚 💸 📽 🕬 🖨 👄	107 + (32) = 73
	$1111_{111}1111111100000 = 00000000000000000000$
Explorer Layers	Time Os 0.5ns 1ns 1.5ns 2ns 2.5ns 3ns 3.5n
He FullAde@74 Sum15	
HillAdde@/5 FullAdde@76 FullAdde@78 FullAdde@78	
H→ FullAdde@79 FullAdde@80 FullAdde@81 FullAdde@81 36 36	
FullAdde@82 FullAdde@83 FullAdde@84	
FullAdde@85 FullAdde@86 FullAdde@87	
	0
	0
- ▲ A14 - ▲ A15 - ● B0	
NOTHING SELECTED SIZE: 184.5 x 125.5 TECH: schematic	(-53, 112)

Figure 11.5: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)



Figure 11.6: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (107 + (- 32) = 75)

😲 Electric		– O X
File Edit Cell Export View	v Window Tools Help	$16 \pm (-28) = -12$
🔁 🗟 📐 🖑 🔍 🌽	井 0.5 📑 📑 🐚 💸 🔹 🎥 🔶 👄 👄	10 + (-20)12
Simulation of sipple conved	0000010000 + 11	11111111100100 = 11111111111110100
Explorer Layers	₩₩ ₩ ₩ ₩ ₩ ₩ ₩ ₩	Time Os 1ns 2ns 3ns 4ns 5ns 6ns
FullAdde@73	¹ Input: A15 ^{× □ ∞ ∞}	0
FullAdde@76 FullAdde@78 FullAdde@79	²Input: A14 ^{× □ ¥}	0
FullAdde@80 FullAdde@81 FullAdde@82 FullAdde@83	³ A13 Input: A13 ^{× □ × ∞}	0
FullAdde@84 FullAdde@85 FullAdde@86	⁴ ⁴ ⁴ ¹² Input: A12 ^{× □ ∞ ∞}	0
FullAdde@87 FullAdde@88 FullAdde@89	^s A11 Input: A11 ^{× □ ×} ℤ	0
• A1 • A2 • • A3	⁶ Input: A10 ^{× □ ∞ ∞}	0
• A4 • A5 • A6 • A7	⁷ / _{A9} Input: A9 × • × • × • × • × • × • × • × • × • ×	0
• A8 • • A9 • • A10	å Input: A8 × ■ × ■ × ■	0
A11 A12 A13 A14	[°] Input: A7 × □ × ≭	0
A15 B0		
NOTHING SELECTED SIZE:	104.3 x 123.3 TECH: SCREMAUC	(-4/.5, 213.5)

Figure 12.1: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)



Figure 12.2: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)

😲 Electric			– 🗆 X
<u>File Edit C</u> ell Export <u>V</u> iew	<u>W</u> indow <u>T</u> ools <u>H</u> elp	$16 \pm (-28) = -12$	
👌 🗟 📐 🖑 Q 🔯 🧈	拱 0.5 號 👎 🖪 🐚 💸 🕸 🐲 🔶 👘	10 + (-20)12	
Simulation of sipple converdence Components	10000010000 + 11	111111111100100 = 11	.1.1111111.0.100 🍱
Explorer Layers	₽ ዞ◀■▶ዞ▲▼	Time 0s 1ns 2ns	3ns 4ns 5ns 6ns
FullAdde@73	[™] Input: B15 ^{× □ ∞}		1
FullAdde@76 FullAdde@78 FullAdde@78 FullAdde@79 FullAdde@80	^{¹9} Input: B14 ^{× □ ⋊} X		1
FulAdde@81 FulAdde@82 FulAdde@83	²⁰ Input: B13 ^{× □ ×}		1
FullAdde@84	²¹ Input: B12 ^{× □ ×}		1
FullAdde@88	²² Input: B11 ^{× •}		1
A1 A2 A3 A4	²³ Input: B10 ^{× □ ×}		1
A5 A6 A7	²⁴ Input: B9 × • × • × •		1
• A8 • A9 • A10	²⁵ Input: B8 × □ × ∞		1
- • A12 - • A13 - • A14	²⁶ Input: B7 × 🖬 💥 🕷		1
A15 B0	27 × 🖬 💥 🕱		· · · · · · · · · · · · · · · · · · ·
NOTHING SELECTED SIZE: 1	84.5 x 125.5 TECH: schematic		(-217, 290.5)

Figure 12.3: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)



Figure 12.4: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)

🙂 Electric		-	o x
<u>File E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u> ie	ew <u>W</u> indow <u>I</u> ools <u>H</u> elp 16	$(\pm (-28)12)$	
🔁 🗟 📐 🖑 🔍 🏹	• 🗮 0.5 🗮 📑 🖪 🖹 🎕 🕿 😭 🔶 🛋 🗖 🗖 🗸	+ (-20)12	
Simulation of sipple converted to the co	<u> 1111 000000000 + 1111</u>	.1131111100100 = 111311111111000000000000	L00 ^{° 💌}
Explorer Layers	∰ Ø K K ■ ▶ H ▲ ▼ Time	0s 1ns 2ns 3ns 4ns 5ns	6ns
FullAdde@73	34 × □ ⋈ ∭ sum15 Output: Sum15	Delay	1
FullAdde@76 FullAdde@78 FullAdde@79	³⁵ × □ ⋈ ₩ sum14 Output: Sum14	Delay	1
FullAdde@80	36 · × □ × ▓ Sum13 Output: Sum13	Delay	1
FullAdde@84	³⁷ × □ × ℤ × ℤ × ℤ	Delay	1
FullAdde@88	³⁸ × □ × ≋ × ™ ×	Delay	1
• A1 • A2 • A3	³⁹ · × □ × ℤ × ℤ × ℤ	Delay	1
	⁴⁰ ' × □ ⋈ ૠ sum9 Output: Sum9	Delay	1
	41 '× □ ½ ૠ suma Output: Sum8	Delay	1
A11 A12 A13 A14	42 × □ 涎 灑 sum ⁷ Output: Sum7	Delay	1
- • A15 - • B0	43 × 🗆 💥 💥		v
NOTHING SELECTED SIZE	: 184.5 x 125.5 TECH: schematic		(-47.5, 213.5)

Figure 12.5: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)

🙁 Electric						o x
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u>	jew <u>W</u> indov	v <u>I</u> ools <u>H</u> elp	16	$\pm (28) = 12$		
i 🚵 🗟 🖡 🖑 Q. 🔯 .			** TO	+ (-20)12		
Simulation of cipple corry Components	000	000010000 +	1111	111111100100 =	- 111111111111010)0 💌
Explorer Layers	ti a		Time	0s 1ns 2ns	3ns, 4ns, 5ns,	6ns
Signals		Out-out- Cu	0	Delay	<u></u>	1 ^
FullAdde@74	Sum8	Output: Su	mð			
FullAdde@75	42	×	■ 💥 🐹	Delevi		1
FullAdde@78	Sum7	Output: Su	m7	Delay		
FullAdde@79	43	' × .	□ 💥 💥			
FullAdde@81	Sum6	Output: Su	m6	Delay		1
FullAdde@83	44	X	▶ 💥 💥			
FullAdde@84	Sum5	Output: Su	m5	Delay		1
FullAdde@86	45	X	. 💥 🐹			
FullAdde@88	Sum4	Output: Su	m4	Delay		1
A0	46	X	₩	1		~
- • A1 - • A2	Sum3	Output: Su	m3			0
- • A3	47	X	₩			
- • A5	Sum2	Output: Su	m^2	Delay		1
- • A7	48	×	₩ ₩	İ. İ.		~
- • A8 - • A9	Sum1	Output: Su	m1			U
A10	49	×	× ×	1		~
- • A12	Sum0	Output: Su	m0			U
- • A13 - • A14	50	X				
- • A15	Cout	Output: Co	i it			U
NOTHING SELECTED	E: 184 5 x 125	5 TECH: schematic		<u> </u>		(-47.5, 213.5)
ULTRATO OCCUPICO VIL						(

Figure 12.6: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)

🙂 Electric									n x
File Edit Cell Export Vi	iew Window Tools Help 50	272	± 500	-520	967				
🚵 🗟 📐 🖑 📿 -	• 拱 0.5 👯 👎 🔁 🐚 💸 🕿 😭 🔶 🗮 🗲	570	- 505	/ – JZ.					
Simulation of ripple carry Components		000		10011	.01 =	11001	.11011	1001	11
Explorer Layers	≝♬ ዞ◀∎▶⊭≜▼	Time	0s 0.2ns	0.4ns 0.6ns	0.8ns 1ns	s 1.2ns 1.4ns	1.6ns 1.8ns	2ns 2.2ns	2.4ns
E FullAdde@73	¹ Input: A15 ^{× •}								1
FullAdde@76	² Input: A14 ^{× •}	ŧ.							1
FullAdde@80	³ Input: A13 ^{× •}	ŧ.							0
FullAdde@84	⁴ Input: A12 ^{× •}	¢.							0
FullAdde@88	⁵ Input: A11 ^{× •}	ŧ.							1
- • A1 - • A2 - • A3	⁶ Input: A10 ^{× •}	¢.							1
	⁷ Input: A9 × • × •	¢.							0
- • A8 - • A9 - • A10	Å Input: A8 × □ 💥	ŧ.							0
• A11 • A12 • A13 • A14	[*] Input: A7 [×] • •	¢.							1
		¢							(DIE E 177)
NOTHING SELECTED SIZ	E: 104.5 X 125.5 TEUR: SUIRINATIC								(213.5, 137)

Figure 13.1: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)



Figure 13.2: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

🙂 Electric					– 🗆 ×
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u> i	ew <u>W</u> indow <u>T</u> ools <u>H</u> elp 5	272 + 52	9 = 52967		
🔁 🗟 📐 🖑 📿 –	• 拱 0.5 拱 📑 📑 🐚 💸 📽 😭 🔶 🗯 🎜	-570 - 50	5 - 52507		
Components			0.1001101		011100111 💌
Explorer Layers	≝₿ н∢∎≻н≜ऱ	Time Os 0.2ns	s 0.4ns 0.6ns 0.8ns	1ns 1.2ns 1.4ns 1.6ns	1.8ns 2ns 2.2ns 2.4ns
E FullAdde@73 € FullAdde@74 FullAdde@75	[™] Input: B15 ^{× ■ ≫}	X			0
FullAdde@76 FullAdde@78 FullAdde@79	¹⁹ Input: B14 ^{× □ ≫}	X			0
FullAdde@80	²⁰ Input: B13 ^{× ■ ≫}	X			0
€ FullAdde@84 € FullAdde@85 € FullAdde@86	²¹ Input: B12 ^{× ■ ≫}	X			0
FullAdde@87	²² Input: B11 ^{× □} ×	X			0
• A1 • • A2 • • A3	²³ Input: B10 ^{× •}	<u>×</u>			0
	²⁴ Input: B9 × • ×	X			1
- • A8 - • A9 - • A10	²⁵ Input: B8 × ■ ≫	<u>×</u>			0
• A11 • A12 • A13 • A14	²⁶ Input: B7 × • ×	X			0
- • A15 - • B0	27 🗙 🖬 💥	*			v
NOTHING SELECTED SIZE	E: 184.5 X 125.5 TEUH: SCREMATIC				(215.5, 137)

Figure 13.3: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)



Figure 13.4: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

😍 Electric						– 🗆 X
<u>File Edit Cell Export V</u>	jew <u>W</u> indow <u>I</u> ools <u>H</u> elp 5	272	2 + 589 - 5296	7		
👌 🗟 📐 🖑 Q 🔀 ,	🔎 拱 0.5 🗮 📑 📑 🐚 💸 🕿 🎥 🔶 🗩 🗲	.570	- 505 - 5250	,,		
Simulation of ripple care Components)000	00100100110	1 = 11001) <u>111 </u>
Explorer Layers	≝♬ ዞ◀■▶ዞ▲▼	Time	0s 0.2ns 0.4ns 0.6ns 0.8	ins 1ns 1.2ns 1.4ns	1.6ns 1.8ns 2ns	2.2ns 2.4ns
E JUIN SIGNALS ▲	34 × ■ ¾ Sum15 Output: Sum1	x 5	Delay			1
FullAdde@76 FullAdde@78 FullAdde@79 FullAdde@80	sumi₄ Output: Sum14	¥ 4	Delay			1
FullAdde@81	³⁶ × ■ × Sum13 Output: Sum13	蒸 3				0
	sum12 Output: Sum12	<u>×</u>				0
FullAdde@88	³⁸ × ∎ ¥ sum1 Output: Sum1	滅 1	Delay			1
• A1 • A2 • • A3	³⁹ × ■ × ■ × ■ ×	X	Delay			1
- • A5 - • A6 - • A7	sum ⁹ Output: Sum ⁹	X	Delay			1
- • A8 - • A9 - • A10 - • A11	suma Output: Sum8	X				0
- • A12 - • A13 - • A14	sum ⁷ Output: Sum7	*	Delay			1
NOTHING SELECTED SIZ	43 X IZ5.5 TECH: schematic	*				(215.5, 137)

Figure 13.5: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

😨 Electric						- 0 X
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u>	jew <u>W</u> indow <u>I</u> ools <u>H</u> elp	52378	+589 = 52	967		
i 🚵 🗟 📐 🖑 Q 🔀 .	🔎 拱 0.5 🚃 📑 📑 💽 🔆 📽 🕬 ቀ	* * * * * * * * * * * * * * * * * * *	1 303 32			
Simulation of ripple care Components	ŢŖĊ ŴŨŨ1 <u>10</u> 10	+ 00000		101 = 1100	11101110	<u>)0111 💌</u>
Explorer Layers	≝♬₩◀■▶₦▲▼	Time	0s 0.2ns 0.4ns 0.6n	s 0.8ns 1ns 1.2ns 1.4	ns 1.6ns 1.8ns 2ns	2.2ns 2.4ns
FullAdde@73	sums Output: S	um8				<u> </u>
FullAdde@75	42	× 🗆 💥 🐹	Deleve			
FullAdde@76	sum7 Output: S	um7	Delay			1
FullAdde@79	43	🗙 🖬 💢 麗	Delay			1
FullAdde@81	sume Output: S	um6	Delay			L
FullAdde@83	44	× 🖬 💓 🐹	Delay			1
FullAdde@85	sums Output: S	um5	Delay			
FullAdde@86	45	🗙 🗆 💥 🐹				0
FullAdde@88	sum4 Output: S	um4				
- • A0	46	🗙 🖬 📈 🌋				0
- • A1	suma Output: Si	um3				
- + A3 - + A4	47	× 🗆 💓 躧	Dolov			1
- • A5	sum2 Output: SI	um2	Delay			1
- • A7	48	×□ズ翼	Dolov			1
• A0	Sum1 Output: SI	um1	Delay			L
A10	49	× □ 💥 🕱	Delay			1
- • A12	sumo Output: Si	um0	Delay			L
- • A14	50	× □ 💥 🐹				
- • A15 - • B0 v	Cout Output: Co	out				U .
NOTHING SELECTED SIZ	ZE: 184.5 x 125.5 TECH: schematic					(215.5, 137)

Figure 13.6: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

😻 Electric	
File Edit Cell Export View Window Tools Help	-10000) = -10071
🔁 🖥 📐 🖑 🤇 🍠 🛲 0.5 🧮 👎 🛅 🐚 🎇 📽 😭 🔶 🗮 🔦 🏧 🍎	10000/ 100/1
Simulation of ripple carry adders 15-Bit-Adder (sch)	L000111110000 = 1101100010101001
Explorer Layers	0s 0.1ns 0.2ns 0.3ns 0.4ns 0.5ns 0.6ns 0.7ns 0.8ns 0.9ns 1ns 1.1ns 1.2ns 1.3ns 1.4ns 1.5ns 1.6ns 1.7ns 1.8ns 1.
FullAdde@74	1
	1
FullAdde@79	_
	1
	i
	1
FullAdde@87 FullAdde@88 5	
	1
	1
→ A11	
	1
	v
NOTHING SELECTED SIZE: 184.5 x 125.5 TECH: schematic	(-114, 215.5)

Figure 14.1: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)



Figure 14.2: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)

😢 Electric	
Eile Edit Cell Export View Window Iools Help	+(-10000) = -10071
🛛 🚵 🗟 📐 🖑 🔍 🔎 🗰 0.5 🗮 👎 🛅 🐚 💸 📽 😭 🗰 🔧 🖝 🌧	/ (-10000) = -10071
Simulation of ripple capy addets 15-Bit Adda (Sch)	1011000111110000 = 1101100010101001
	Time Os 0.1ns 0.2ns 0.3ns 0.4ns 0.5ns 0.6ns 0.7ns 0.8ns 0.9ns 1ns 1.1ns 1.2ns 1.3ns 1.4ns 1.5ns 1.6ns 1.7ns 1.8ns 1.
Fulade@74 Fulade@74 Fulade@74	
Fullade@82 Fullade@82 Fullade@82	0
FulAde@84 FulAde@88 FulAde@886 FulAde@886	
	O
	0
◆ A11 ◆ A12 ◆ A13 ◆ A14 ²⁶ Input: B7 × □ ※灑	
▲ A15 → B0 ✓	· · · · · · · · · · · · · · · · · · ·
NOTHING SELECTED SIZE: 184.5 x 125.5 TECH: schematic	(-114, 215.5)

Figure 14.3: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)



Figure 14.4: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)

● Electric - □ >	
$\frac{[\text{Ele } \underline{f} dit \underline{c} ell \underline{f} \underline{x} port \underline{v} ew \underline{W} indow \underline{I} ools \underline{H} elp (\underline{-71}) \pm (\underline{-10000}) - \underline{-10071}$	
● □ ● □ へ 図 ● 囲 • □ = ■ ■ ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ● ●	
© Simulation of risplay carry address 11 to 1, 1001 + 1101, 1000 carr 1 110000 = 1, 100, 110001010101001	x
Explorer Layers 🖽 🗷 H 🗲 🖬 N A 🖛 V H A 🖛 Time 0s 0.1ns 0.2ns 0.3ns 0.4ns 0.5ns 0.6ns 0.7ns 0.8ns 3	
at x a x a x a x a x a x a x a x a x a x	^
FulAdde@76 FulAdde@78 FulAdde@78 Sum14 Output: Sum14 Delay 1	
FulAdde@81 FulAdde@82 FulAdde@83 FulAdde@83 FulAdde@83 FulAdde@83	
FullAdde@84 37 × □ ≥ ∞ FullAdde@85 Sum12 Output: Sum12 Delay	
TulAdde@89 ■ AUXAdde@89 ■ AUXA	
$\begin{array}{c c} & A_1 \\ \hline & A_2 \\ \hline & A_3 \end{array} \end{array} \xrightarrow{39} \begin{array}{c c} \times \square \not \times \cancel{3} \\ \hline & Sum10 \\ \hline & Output: Sum10 \\ \hline & Output: Sum10 \\ \hline \\ \end{array}$	
AA AAS AAS AAZ AAS Sum9 Output: Sum9 Output: Sum9	
AB AB AB AB AD AD	
All Al2 Al3 Al4 Sum ⁷ Output: Sum ⁷ Delay 1	
▲ A15 ▲ 3 × □ ⋈ 波 ■ B0 ✓ Image: A15	v .5.5)

Figure 14.5: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)



Figure 14.6: IRSIM Waveforms of Schematic Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)

Section 6: Electric Layout:

We created a layout of the 16-Bit Ripple Carry Adder by combining 16 Full Adders (Figure 6) together. It was combined by connecting the Cout of the Full Adder to the Cin of the next Full Adder. Figure 15 shows the layout design that was built using Electric of the 16-Bit Ripple Carry Adder. There's an overview and a zoomed version of the layout since the overview isn't clear enough. If there's any need for any justifications refer to Figure 6, Full Adder.

Figure 15.0 to 15.5 shows an overview and slowly zooming into the layout.

Figure 15.6 shows the left sides of the layout. It's basically a Full Adder.

Figure 15.7 shows the part of the layout that gets repeated from 1 to 14, from left to right. Its Full Adders connected together.

Figure 15.8 shows the right part of the layout. It's still a Full Adder.

Figure 16 shows the Design Rule Check (DRC) and Well Check that was performed on the layout; it indicates that there were no errors or warning with the layout.



Figure 15.0: Layout Design of a 16-Bit Ripple Carry Adder Overview (Landscape)



Figure 15.1: Layout Design of a 16-Bit Ripple Carry Adder Overview Zoomed (Landscape)



Figure 15.2: Layout Design of a 16-Bit Ripple Carry Adder Overview Zoomed (Landscape)



Figure 15.3: Layout Design of a 16-Bit Ripple Carry Adder Overview Zoomed (Landscape)



Figure 15.4: Layout Design of a 16-Bit Ripple Carry Adder Overview Zoomed (Landscape)



Figure 15.5: Layout Design of a 16-Bit Ripple Carry Adder Overview Zoomed (Landscape)



Figure 15.6: Layout Design of a 16-Bit Ripple Carry Adder Zoomed Left Side (Landscape)



Figure 15.7: Layout Design of a 16-Bit Ripple Carry Adder Zoomed From 1-14 (Landscape)



Figure 15.8: Layout Design of a 16-Bit Ripple Carry Adder Zoomed Right Side (Landscape)

😟 Electric Messages

Figure 16: Design Rule Check (DRC) and Well Check of a 16-Bit Ripple Carry Adder Layout Design

Section 7: LTSPICE for Electric Layout:

After creating the layout design of the 16-Bit Ripple Carry Adder, waveforms were created using LTSPICE. The waveforms were created by using Spice Code to initialize our VDD, GND, and our 33 inputs, A (0-15), B (0-15), and Cin. It was also used to produce the type of analysis we want; in this case, we used a transient analysis, which goes as far as 80ns.

The Spice Code that we wrote is shown on Figure 9; it's the same code that was used for the Electric Schematic. In addition, Table 6 shows the inputs in binary and the outputs that was obtained from both computation and LTSPICE.

	First Computation	Second Computation	Third Computation	Fourth Computation
Input: A	-32	-28	52378	-71
	(1111111111100000)	(1111111111100100)	(1100110010011010)	(1111111110111001)
Input: B	107	16	589	-10000
	(000000001101011)	(000000000010000)	(0000001001001101)	(1101100011110000)
Output:	75	-12	52967	-10071
Expected	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)
Sum				
Output:	75	-12	52967	-10071
LTSPICE	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)
Sum				

Table 6: Inputs and Outputs of the Computations (Layout)

✓ LTspice XVII - [16-Bit-Adder spi] ※ Eile View Plot Settings Simulation IF ▶ #□ 국가 # ○ < < < < > 18 bit ▶ #□ 국가 # ○ < < < < > 18 bit ▶ Bit-Adder.spi ■ 18-Bit-Adder.spi	bols Window Help Na kl⊉ / ৬৩ ২ ቀ 3 호마 원 ৩ ৩ ৫ ৯೧. –	V(a15)	52378	-71
1.7v-Input: A15 0	0	V(a14)	1	1
^{3.3V} ^{1.7V-} Input: A14 0	0	V(a13)	1	1
^{3.3V} ^{1.7V} Input: A13 (0		0	1
^{3.3V} ^{1.7V-} Input: A12 0	0		0	1
^{3.3V} ^{1.7V} Input: A11 0	0	V(a11)	1	1
^{3.3V} ^{1.7V} Input: A10 0	0	V(a10)	1	1
^{3.3V} ^{1.7V} Input: A9 0	0	V(d9)	0	1
^{3.3V} 1.7V-Input: A8 0	0	V(a8)	0	1
^{3.3V} ^{1.7V} Input: A7 0	0	V(a7)	1	1
Ons 8ns	16ns 24ns 32ns	40ns	48ns 56ns	64ns 72ns 80ns

Figure 17.1: LTSPICE Waveforms of Layout Design of 16-Bit Ripple Carry Adder (A15-A7)

ダ LTspice XVII - [16-Bit-Adder.spi] Elle View Plot Settings Simulation Iools Window He アメリアンズ していたい マントロント	elp J x p-20 c c c c a a m		- Ø	× 2 x
▶ 16-Bit-Adder.spi				
^{3.3V-} 1.7V- Input: A6 1	0		0	
^{3.3V} 1.7V- Input: A5 1	0		1	
^{3.3V} 1.7V-Input: A4 0	1		1	
^{3.3V} 1.7V- 0.0V	0		1	
^{1.0mV} Input: A2 0.0mV 0	0		0	
^{3.3V} 1.7V-Input: A1 1	0		0	
^{3.3V} 1.7V-Input: A0 <u>1</u>	0	0	1	
1.0mV 1 pout: Cip -		V(cin)		
-1.0mV- 0ns 8ns 16ns	0 24ns 32ns	40ns 48ns	66ns 64ns 72ns	80ns

Figure 17.2: LTSPICE Waveforms of Layout Design of 16-Bit Ripple Carry Adder (A6-A0)

Itspice XVII - [16-Bit-Adder.spi] Eile View Plot Settings Sin lation pols P 코 데 국가 프 은 Q Q 및 Lacid 관 관 호구· · · · · · · · · · · · · · · · · · ·	Window Help #/->=>==================================	V(b15)	589	-10000	× . // ×
^{3.3V} ^{1.7V-} Input: B15 <u>1</u>	1	V(b14)	0	1	
^{3.3V} ^{1.7V-} Input: B14 <u>1</u>	1	V(b13)	0	1	
^{3.3V} ^{1.7V-} Input: B13 <u>1</u>	1	V(b12)	0	0	
^{3.3V} 1.7V-Input: B12 <u>1</u>	1	V(512)	0	1	
^{3.3V} 1.7V-Input: B11 <u>1</u>	1	V(511)	0	1	
^{3.3V} 1.7V-Input: B10 <u>1</u>	1	1((50)	0	0	
^{3.3V} 1.7V-Input: B9 <u>1</u>	1	V(b3)	1	0	
^{3.3V} 1.7V-Input: B8 <u>1</u>	1	V(D8)	0	0	
^{3.3V} ^{1.7V} Input: B7 1	1	v(b/)	0	1	
0ns 8ns 16	Sns 24ns 32ns	40ns	48ns 5	56ns 64ns 72ns	80ns

Figure 17.3: LTSPICE Waveforms of Layout Design of 16-Bit Ripple Carry Adder (B15-B7)

Input: B6	_	V(b6)	
1	1	1	1
-		V(b5)	
Input: B5 <u>1</u>	1	0	1
		V(b4)	
Input: B4 ()	0		
		V(b3)	
Input: B3 ()	0	1	0
	1	V(b2)	
Input: B2 U			U
Input: B1	0	V(b1)	0
0	U	U	U
	0	1	
	U		U

Figure 17.4: LTSPICE Waveforms of Layout Design of 16-Bit Ripple Carry Adder (B6-B0)

LTspice XVII - [16-Bit-Adder.sp.] LTspice XVII - [16-Bit-Adder.sp.] File View Plot Settings Simu fil P # 및 귀가 취 및 및 및 것 및 및 및 및 및 및 및 및 및 및 및 및 및 및 및	on Tols Window Hel 5 관리 관려 / 스 수 印 २ ≑ 3	p ☆⊅-80 500000 m	2	-52	296	7 ·	-10	07	× . * *
3.6V Output: Sum 1	.5			V(sum15)					
1.7V-			1		- 1		γ	1	
^{0.3V} Output: Sum 1	4			V(sum14)					
1.7V=			1		1			1	
^{0.3V} Output: Sum 1	3			V(sum13)					
1.7V-)		1		0			0	
3.6V Output: Sum 1	.2			V(sum12)					
1.7V-)		1		0			1	
3.6V Output: Sum 1	1			V(sum11)					
1.7V-			1		- 1			1	
3.6V Output: Sum 1	0			V(sum10)					
1.7V-)		1		1			0	
3.6V Output: Sum 9		· · · · · · · · · · · · · · · · · · ·		V(sum9)			•		
1.7V-)		1		1			0	
^{3.6v} Qutput: Sum 8				V(sum8)				_	
1.7V-			1		0		~	0	
3.6V Output: Sum7				V(sum7)					
1.7V-			1		1		V	1	
-0.3V Ons 8ns	16ns	24ns	32ns	40ns	48ns	56ns	64ns	72ns	80ns

Figure 17.5: LTSPICE Waveforms of Layout Design of 16-Bit Ripple Carry Adder (Sum15-Sum7)



Figure 17.5: LTSPICE Waveforms of Layout Design of 16-Bit Ripple Carry Adder (Sum6-Sum0)

Section 8: IRSIM for Electric Layout:

After creating the layout design of the 16-Bit Ripple Carry Adder, waveforms were created using IRSIM. Theses waveforms were created by configuring the inputs, A and B, so it could test certain computations. The computations we tested are the same as what's shown in Table 6 (same values as the LTSPICE), also shown on Table 7. When setting in values for the inputs, the output would automatically update based on the inputs. We were able to verify that the waveforms obtained from IRSIM matches on Table 7.

Figure 18, 19, 20, and 21 shows the IRSIM waveforms for the 16-Bit Ripple Carry Adder.

	First Computation	Second Computation	Third Computation	Fourth Computation
Input: A	107	16	52378	-71
	(000000001101011)	(000000000010000)	(1100110010011010)	(1111111110111001)
Input: B	-32	-28	589	-10000
	(111111111100000)	(1111111111100100)	(0000001001001101)	(1101100011110000)
Output:	75	-12	52967	-10071
Expected	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)
Sum				
Output:	75	-12	52967	-10071
IRSIM Sum	(000000001001011)	(1111111111110100)	(1100111011100111)	(1101100010101001)

Table 7: Inputs and Outputs of the Computations (Layout)

😍 Electric		o x
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u> i	$\frac{107 + (-32)}{107 + (-32)} = 75$	
👌 🗟 📐 🖑 🔍 🔁 -	▶ 冊 05 票 〒 国 観 観 惶 艸 幸 奋 エン・・ (ジン / ー・ / ジ	
Simulation of Tipple any Components	CICCOTIOLOII + 1111111111100000 = 000000000000000000	11 🗖
Explorer Layers	111 2 N	4ns
	¹ Input: A15 ^{× □ × ∞}	0 [^]
• A3 • A4 • A5		0
	^³ Input: A13 ^{× □ ∞ ∞}	0
- • A10 - • A11 - • A12	AI2 Input: A12 ^{× □ × ∞}	0
• A13 • A14 • A15	^s Input: A11 ^{× □ × ∞}	0
- • B1 - • B2 - • B3	ÅioInput: A10 ^{× □ ∞ ∞}	0
	⁷ Input: A9 × B × M	0
• B8 • • B9 • • B10	åInput: A8 × ■ × ∞ × ■ × ∞ × ■ × ∞ × ■ × ∞ × ∞ × ∞	0
• B11 • B12 • B13 • B14	[°] Input: A7 ^{× □ × ∞} [×]	0
- + B15 - + Cin +		~
NOTHING SELECTED SIZ	ZE: 5962.5 x 151 TECH: mocmos (scale=175.0nm,toundry=MOSIS)	(-119.5, 70.5)

Figure 18.1: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)



Figure 18.2: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)

🙁 Electric		– 🗆 X
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u>	$\underline{\text{View } \underline{\text{Window } Iools } \underline{\text{Help}} = 107 \pm (-32) \pm 75$	
🔁 🖶 📐 🖑 📿 .	- 弗 0.5 照 👎 🖪 🖹 総 😫 🛊 🗣 🕿 🎴 🕇 🕇 🕄 🖉	
Simulation of Tipple rany Components	00001101011 + 111111111111110000	0 = 0000000010010011
Explorer Layers	- 班 ダ N ◀ ■ ▶ N ▲ マ Time Os 0.5ns 1ns	1.5ns 2ns 2.5ns 3ns 3.5ns 4ns
	¹⁸ Input: B15 ^{× □ × ∞}	1
- • A3 - • A4 - • A5	¹⁹ Input: B14 ^{× □ × ∞}	1
	²⁰ Input: B13 ^{× □ ※}	1
• A10 • A11 • A12 • A13	²¹ Input: B12 ^{× □ ★ ★}	1
- • A14 - • A15 - • B0	²² Input: B11 ^{× • × ×}	1
- • B1 - • B2 - • B3	²³ Input: B10 ^{× □ ≫ ∞}	1
• • • • • • • • • • • • • • • • • • •	²⁴ Input: B9 × □ ≥ 2 2	1
• 88 • 89 • 810	²⁵ Input: B8 × □ ½ ₩	1
B12 B13 B14	²⁶ Input: B7 × □ ≥ 28	1
+ B15 + Cin +		
NOTHING SELECTED SIZ	SIZE: 5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=MOSIS)	(-119.5, 70.5)

Figure 18.3: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)

🙂 Electric										-	D X
<u>F</u> ile <u>E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u>	iew <u>W</u> indow <u>T</u> ools <u>H</u> elp	10	7 + (-	221 -	- 75						
👌 🗟 📐 🖑 Q 🔯 .	🔎 🌐 0.5 🚃 👎 📑 💽 💸 📽 😭 🗰 👄 👁	° TO	/ I _ [-	52)-	- / 5						
Simulation of Topte any	000001101011 +	1111	1111	1110	0000)0 =	000	0000	001	0010	11 💌
Explorer Layers		Time	0s	0.5ns	1ns	1.5ns	2ns	2.5ns	3ns	3.5ns	4ns
E-JACK SIGNALS		w 38									^
- • A1 - • A2	Binput: B6										1
- • A3 - • A4	²⁸ Input· B5 × •	× 100									1
- • A5 - • A6	впрастьз		_ _				i				_
• A7 • A8	²⁹ Input: B4 × •	× <u>ж</u>									0
- • A9		1 10 mt									<u> </u>
- • A11 - • A12	Binput: B3	莱莱									0
- • A13	31	w 36					i				~
A14 A15 B0	[■] Input: B2	, Jun									0
- + B1	32	× 💥	i —				i i				^
	BI Input: B1										U
B5	³³ Incourts DO ×	★ 麗									
- • B6											U
- • B8	35 × □	56 56	i =				i				~
- • B9	sum15 Output: Sum	15									0
- + B11			1								
• B12 • B13	Sum14 Output: Sum	1/									0
- + B14			1								-
	37 🗙 🗖	突 蒸									~
NOTHING SELECTED SIZ	ZE: 5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=	MOSIS)									(-119.5, 70.5)

Figure 18.4: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)

😲 Electric		
<u>File E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u>	<u>View Window Iools Help</u> $107 + (-32) = 75$	
👌 🗟 📐 🖑 📿	■ # # 05 ;;; = 1	
Simulation of Topte rany Components	QQQQQQ1 + 111111111111100000 = 000000000000000	001011 💌
Explorer Layers		3.5ns 4ns
A0	[∧] 35 × □ ∞ 2%	
- • A1	sum15 Output: Sum15	U
- + A2 - + A3		
- • A4	Curtout: Sum 14	0
- • A5		
- • A7		
- • A9		U
+ A10	38 🛛 🖌 🖬 💥 💥	0
- • A12		<u> </u>
- • A13	39 × □ 汝 潔	
- • A15		0
- + B2	Output: Sum 10	()
- • B3		
- • B5		0
- + B7		
- • B8		
- + B10		<u> </u>
- • B11	43 * • • • • • • • • • • • • • • • • • •	<u> </u>
- • B13	Sum7 Output: Sum7	0
- + B14 - + B15		
- • <u>Cin</u> v		~
NOTHING SELECTED SIZ	SIZE: 5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=MOSIS)	(-119.5, 70.5)

Figure 18.5: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)

🙂 Electric											-	□ ×
<u>File E</u> dit <u>C</u> ell E <u>x</u> port	t <u>V</u> iew <u>W</u> inc	ow <u>I</u> ools <u>H</u> elp	-	107	7 + (-32)	= 75						
👌 🗟 📐 🖑 🔍	🔀 🧢 拱 0.	s 📰 👎 🔁 💽 💥 🕿 🕬	*****	107	1 (32)	- / 5						
Simulation of Tipple		00110101	1 + 11	11	1111111	0000) = 00	000	0000	0010	010	11 🔼
Explorer Layer	s 🕂 a			T	Ios I0 5ns	1ns	1 5ns	2ns	2 5ns	3ns	3 5ns	4ns
SIGNALS				i ime			1.010		2.010		0.010	- <mark>n</mark> -,
- • A0	Sum8	Output:	Sum8									
- • A2	43		×□ > З 🦋 🔣									0
- + A3	Sum7	Output	Sum7									0
- + A5	44	Output.										
A6	Sum6	Output	Sum6		Delay							1
- • A8	Sumo	Output.	Sumo									-
A9	45		× □ 舛 漢					i i				
- + A11	Sum5	Output:	Sum5									0
A12	46		×□灑					1				0
- • A14	Sum4	Output	Sum4									U
- + A15	47	output	XIX					1				
- + B1	Sum3	Output	Sum2		Delav							1
- • B3	40	Output.	Juiij									-
- • B4	48	Ott .										0
• B5	Sum2	Output:	Sumz									<u> </u>
- + B7	49		🗙 🖬 📈 🎇		Dolov							1
- • B9	Sum1	Output:	Sum1		Delay							
● B10	50		🗙 🗆 💓 🐹		Delau			1				
• B12	Sum0	Output	SumO		Delay							1
● B13	51	output.										_
- + B15	Gut	Output	Cout		Delay			1				1
Cin	✓ Cout	<u> </u>	Cout					<u> i </u>				
NOTHING SELECTED	SIZE: 5962.5 x	151 TECH: mocmos (scale=175.	0nm,foundry=MOSIS)									(-119.5, 70.5)

Figure 18.6: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (107 + (-32) = 75)

😃 Electric								– 🗆 X
<u>File Edit C</u> ell Export <u>V</u> ie	w <u>W</u> indow <u>T</u> ools <u>H</u> elp	16 +	(_28)	= -12				
🔁 🗟 📐 🖑 🔍 🎑 🧢	• 🗰 0.5 🚃 📑 📑 🐚 💸 📽 🞥 🔶 🔿 👄 👘	TOI	(20)	- 12				
Simulation of cipple corrections	00000010000 + 11	111		11001	00 = 1	1111		110100
Explorer Layers	≝♂ н∢∎⊁н≜∀	Time Os	0.5ns	1ns 1.5ns	2ns 2.5	ins 3ns	3.5ns 4ns	4.5ns 5.5ns
• A0 • A1 • A2	¹ Input: A15 ^{× •}							0
• A3 • A4 • A5	² Ai4 Input: A14 ^{× • •}							0
A6 A7 A8 A8	³ Input: A13 ^{× •}							0
A10 A11 A12	⁴ A12 Input: A12^{× □ X X}							0
A13 A14 A15 B0	⁵ Input: A11 ^{× •}							0
• B1 • B2 • B3	¦input: A10 ^{× □ ⋊}							0
B4 B5 B6 B7	⁷ Input: A9 × • × • × *							0
• B8 • B9 • B10	å Input: A8 × □ × ∞							0
	³ Input: A7 × • × ×		_					0
								v
NOTHING SELECTED SIZE:	5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=MOSIS							(177, 2003.5)

Figure 19.1: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (16 + (-28) = - 12)

😃 Electric												-		×
<u>File Edit C</u> ell Export <u>Y</u>	<u>V</u> iew <u>W</u> indow	<u>T</u> ools <u>H</u> elp		16	5 ± 1	281	11)						_
👌 🗟 ト 🖑 Q 🖸	🏓 拱 0.5 🛒	: 🗝 📑 💽 🎗	옷 🕿 🔉 🔶 🗯	*	יזינ	201	12	-						
Simulation of sipple com	0000	0001	0000 +	1111	11112.0	111	1001	LOO =	- 11	1.1.1.1		1101	.00	x
Explorer Layers	11 a M	∢ Ⅲ ≻ н 4	≜ ₹	Time	0s	0.5ns	1ns 1.5	ns 2ns	2.5ns	3ns 3.5	5ns 4ns	4.5ns 5n	is 5.5ns	\$
- • A0 - • A1 - • A2	10 A6	nput:	A6 × □	X									0	^
• A3 • A4 • A5		nput:	A5 × •	× ×									0	
A7 A8 A9	12 A4	nput:	A4 × •	× ×									1	
A10 A11 A12 A13	13 A3	nput:	A3 × •	× ×									0	
- A14 - A15 - B0	14 A2	nput:	A2 × •	× ×									0	
B1 B2 B3 B3	15 A1	nput	: A1 × •	× ×									0	
B5 B6 B7	16 A0	nput	: A0 [×] □	₩ ₩									0	
• B8 • B9 • B10	17 Cin	nput:	Cin [×]	× ×									0	
B12 B13 B14	18 B15	put:	B15 [×] □	※ 派									1	
NOTHING SELECTED SI	19	TECH: mocmo	s (scale=175.0nm.foundr	₩ X									(177, 200	3.5)

Figure 19.2: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (16 + (-28) = -12)

😲 Electric	- 0	×
<u>File Edit C</u> ell Export <u>V</u>	$16 \pm (-28) - 12$	
👌 🗟 📐 🖑 Q 🐼 ,	≠# 5 ;; ₹ 5 ;; ₹ 5 ;; * 6 ; * 6 ; * 6 ; * 7 ; (-20) = -12	
Simulation of vipole corry Components	$\frac{1}{10000010000} + 111111111100100 = 1111111111110100$	x
Explorer Layers	₩ 2 N 4 ■ > N ▲ = Time Os 0.5nş 1ns 1.5nş 2ns 2.5nş 3ns 3.5nş 4ns 4.5nş 5ns 5.5	ns
• A0 • • A1 • • A2	¹⁸ Input: B15 ^{× □} × × 1	^
	¹⁹ Input: B14 ^{× □ × ∞}	
	²⁰ Input: B13 ^{× •} × × 1	
• A10 • A11 • A12	²¹ Input: B12 ^{× B} ×× 1	
	²² Input: B11 ^{× □ × ∞}	
• B1 • B2 • B3	²³ nput: B10 [×] [∞] × [∞] × [∞] 1	
	²⁴ Input: B9 × 🛛 💥 📕 📘	
	²⁵ Input: B8 × 🛛 × 🖓 💥 📘 📘 1	
	²⁶ Input: B7 × □ × ℝ × ℝ × ℝ × ℝ × ℝ × ℝ × ℝ × ℝ × ℝ	-
- • B15 - • Cin v		-
NOTHING SELECTED SIZ	ZE: 5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=MOSIS) (177, 2	003.5)

Figure 19.3: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (16 + (-28) = - 12)

🙁 Electric								– 🗆 X
<u>File Edit C</u> ell Export	<u>V</u> iew <u>W</u> indow <u>T</u> ools <u>H</u> elp	16	$\pm (-28)$	- 12				
👌 🗟 ト 🖑 Q 🐼	🏓 拱 0.5 🚃 👎 📑 🐚 💸 🕸 🕋 🖨 🖷	* то	- (-20)	12				
Simulation of sigple con	00000010000 + 1	.111	1111111	.10010	00 = 1	1.1.1.1.1.	11111	10100
Explorer Layers	≝₽ н∢∎⊁н≜⊽	Time	0s 0.5ns	1ns 1.5ns	2ns 2.5ns	3ns 3.5n	s 4ns 4.	5ns 5.5ns
- A0 - A1 - A2	²⁷ Input: B6 × ■ ×	()X(1
• A3 • A4 • A5 • A6	²⁸ Input: B5 × ■ ≫	(%						1
• A7 • A8 • A9	²⁹ Input: B4 × □ ×							0
A10 A11 A12 A12 A13	Binput: B3 × • *							0
A14 A15 B0	³¹ Input: B2 × ■ *							1
• B1 • B2 • B3 • B4	³² Input: B1 × • ×							0
	³³ Input: B0 × ■ ≫	(% (0
B8 B9 B10	34 × ■ ≫ Sum15 Output: Sum1	· ² / ₂	Delay	/				1
	³⁵ × ■ × Sum14 Output: Sum1	4	Delay	/				1
NOTHING SELECTED	36 × □ ×	(%						(177, 2003 5)

Figure 19.4: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (16 + (-28) = - 12)

🙁 Electric			– 🗆 X
<u>File E</u> dit <u>C</u> ell E <u>x</u> port <u>V</u>	<u>/</u> iew <u>W</u> indow <u>T</u> ools <u>H</u> elp	$16 \pm (-28) = -12$	
👌 🗟 🕨 🖓 🔍 🔀	🔎 拱 0.5 🗮 👎 📑 🐚 💸 📽 😭 🔶 🔿 👄	10 + (-20)12	
Simulation of sipple com	00000010000 + 11	111_{2}	11111110100 🍱
Explorer Layers	≝₽ н∢∎⊁н≜⊽	Time Os 0.5ns 1ns 1.5ns 2ns 2.5ns	3ns 3.5ns 4ns 4.5ns 5ns 5.5ns
→ A0 → A1 → A2	³⁴ × □ ⋈ ₩ Sum15 Output: Sum15	Delay	
• A3 • A4 • A5	35 ' × ▣ ¾ ¥ Sum14 Output: Sum14	Delay	1
A6 A7 A8 A9	36 · × □ ⋈ ₩ Sum13 Output: Sum13	Delay	1
• A10 • A11 • A12	³⁷ ′ × □ ⋈ ⋈ Sum12 Output: Sum12	Delay	1
A13 A14 A15 B0	³⁸ × □ ※駕 Sum11 Output: Sum11	Delay	1
• B1 • B2 • B3	³⁹ ×□涎灑 ^{Sum10} Output: Sum10	Delay	1
■ 64 ■ 65 ■ 66 ■ 67	⁴⁰ × □ ※駕 Sum ⁹ Output: Sum9	Delay	
• B8 • 9 • B10	41 × □ ※ 灑 涎 灑 Sum8 Output: Sum8	Delay	1
• B11 • B12 • B13 • B14	42 × □ 涎 灑 Sum ⁷ Output: Sum7	Delay	1
● B15 ● Cin ✓	43 × 🖬 💥 💥		~
NOTHING SELECTED SIZ	ZE: 5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=MOSIS		(177, 2003.5)

Figure 19.5: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (16 + (-28) = - 12)

😃 Electric											- 0	x i
<u>File Edit C</u> ell Export	t <u>V</u> iew	<u>W</u> indow	<u>T</u> ools <u>H</u> elp		16	+(28) -	12					
👌 🗟 🕨 🖓 🔍 🛛	🖸 🧈 🗦	# 0.5 -	:: 👎 🔁 💽 🛠 🕿 💓 🔻		TO -	- (-20) –	-12					
Simulation of sipple of	ary-add	15/16-Bit		1 + 11	111	111111	00100 -	- 11	1111	1111	11010	∩' 💌
Components	<u>الم</u>	<u>九〇</u>) + TT	T T 1	tain 2.008ns Center	- 00100	- _ _	2.886ns Cente	****		U
Explorer Layers	s 🔛	Ø I	(◀■▶Ы▲ऱ		Time	0s 0.5ns 1ns	1.5ns 2ns	2.5ns	3ns 3.5i	ns 4ns	4.5ns 5ns	5.5ns
+ A0		Sum8	Output: 9	Sum8		Delay						1 ^
- • A1		42		× 🗆 💥 🚟		- •		· · · · ·				
- • A3 - • A4	-	Sum7	Output: 9	Sum7		Delay						1
- • A5		43	- outputt	XDMW								
• A6 • A7		Sum6	Output [.]	Sum6		Delav						1
- • A8 - • A9		44	output	×□关骥								
• A10 • A11	5	Sum5	Output: 9	Sum5		Delay						1
A12		45		🗙 🗆 💥 🐹								
A14	5	Sum4	Output: S	Sum4		Delay						1
- • B0		46		🗙 🖬 💥 麗								
- ● B1 - ● B2		5um3	Output: S	Sum3								0
• B3		47		🗙 🖬 🎽 麗								
- • B5		Sum2	Output: S	Sum2		Delay						1
• B0		48		× 🗆 💥 🕷				1				~
- • B8		Sum1	Output:	Sum1								0
- • B10		49	output					1				
♦ B11 ♦ B12		Sum0	Output:	SumO								υ
- • B13			Output.	Junio								
- + B14 - + B15		50	•	メヨダ薬				i				0
- Cin	~ (Cout	Output: (out								<u> </u>
NOTHING SELECTED	SIZE: 59	62.5 x 151	TECH: mocmos (scale=175.0r	nm,foundry=MOSIS)							(177, 2003.5)

Figure 19.6: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (16 + (-28) = - 12)

🙂 Electric	- 0	×
File Edit Cell Export V	iew Window Tools Help 52378 + 589 - 52967	
👌 🗟 ト 🖑 Q 🖸 .		
Simulation of ripple carry	$\frac{1}{100}$	x
Explorer Layers		2.4
A0 A1 A2	¹ Input: A15 ^{× □ × ×}	^
- • A3 - • A4 - • A5	² Input: A14 ^{× • • × ×}	
- • A7 - • A8 - • A9	³ Input: A13 ^{× • × ×})
- • A10 - • A11 - • A12 - • A13	⁴ Input: A12 ^{× □ × ×} 0	
- • A14 - • A15 - • B0	¹ Input: A11 ^{× • × ×}	
- • B1 - • B2 - • B3	10 hput: A10 ^{× •}	-
	⁷ Input: A9 × B × K C)
	[*] Input: A8 × • × × × × × × × × × × × × × × × × ×)
• B11 • B12 • B13 • B14	[*] Input: A7 × • × × × × 1	-
NOTHING SELECTED	10 X Q X X X X X X X X X X X X X X X X X	5 158)
SIZE SIZE SIZE SIZE		, 200)

Figure 20.1: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)



Figure 20.2: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

😃 Electric		×
<u>File Edit Cell Export V</u>	$\frac{1}{100}$ Liols Help $52378 + 589 = 52967$	
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	²⁰ Input: B13 ^{× □ × X})
- • A10 - • A11 - • A12	²¹ Input: B12 ^{× □ × ×})
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Figure 20.3: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)



Figure 20.4: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

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Figure 20.5: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

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• B11 • B12	Sum0	utput: S	umÔ		Delay					1
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Figure 20.6: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder (52378 + 589 = 52967)

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Simulation of ripple carry_addep=16-Bit Compagence	1-Adder[1av] 1111001 + 11	01100011110000 = 1	101100010101001
Explorer Layers	H ◀ ■ → H ▲ ₹	Time Os 0.2ns 0.4ns 0.6ns 0.8ns 1ns 1	2ns 1.4ns 1.6ns 1.8ns 2ns 2.2ns 2.4ns
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A3 A4 A5 A5 A14	nput: A14 ^{× ••} ***		1
A7 A8 A9 3 A13	nput: A13 ^{× ••} ***		1
4 A10 A11 A12 A12 A12	nput: A12 ^{× •} ***		1
- • A14 - • A15 - • B0	nput: A11 ^{× •• ×} **		1
6 6 82 6 A10	nput: A10 ^{× •} ***		1
	nput: A9 × • × *		1
B8 B9 B10 A8 A8	nput: A8 × • × ×		1
B12 B13 B14 A7	nput: A7 × • • • •		1
• B15 10	× 🗆 💥 💥		v
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Figure 21.1: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)



Figure 21.2: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)

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Simulation of ripple carry		×
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Explorer Layers	Image: Book of the second	2.4ns
• A0 • A1 • A2	¹⁸ Input: B15 ^{× □ ⋊ X}	^
• A3 • A4 • A5	¹⁹ Input: B14 ^{× □ × ×}	
	²⁰ Input: B13 ^{× □} × ∞ × ∞ → ∞ 0	
• A10 • A11 • A12	²¹ Input: B12 ^{× □ × ∞} ↓ 1	
	²² Input: B11 ^{× •} × × · · · · · · · · · · · · · · · · ·	
• B1 • B2 • B3	²² Input: B10 ^{× □ × ∞} 0	
• B5 • • B6 • • • B7	²⁴ Input: B9 × □ ¥ ₩ 0	
• B8 • B9 • B10	²⁵ Input: B8 × □ × ℝ → ∞ ∞ 0	
• B11 • • B12 • • B13 • • B14	²⁶ Input: B7 × B × K	
● B15 ● Cin ✓		~
NOTHING SELECTED SIZE	E: 5962.5 x 151 TECH: mocmos (scale=175.0nm,foundry=MOSIS) (-20:	5, 161.5)

Figure 21.3: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)



Figure 21.4: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)

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Simulation of ripple care Components		1100011110000 = 1	101100010101001
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E-7.7.7. SIGNALS	34 × 口 対 凝		·
- • A1 - • A2	sum15 Output: Sum15	Delay	1
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- • A4 - • A5	sum14 Output: Sum14	Delay	
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- • A11 - • A12	sum12 Output: Sum12	Delay	1
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- • A15	Sum11 Output: Sum11	Delay	
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• B2 • B3	sum10 Output: Sum10		U
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• B6	sume Output Suma		U .
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- • B9			i O
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- • B13	Output: Sum 7	IDelav	1
- • B14			<u> </u>
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Figure 21.5: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)



Figure 21.6: IRSIM Waveforms of Layout Design of a 16-Bit Ripple Carry Adder ((-71) + (-10000) = -10071)

Section 9: Summary of Measurements:

The rise time, fall time, and propagation delay of gates of entire I/O are all shown on the table below, Table 8. It's found that for LTSPICE, the Schematic is faster compared to the Layout; the delay times are less, and it's rise and fall time are shorter. It's also found that for the IRSIM, the Schematic is faster compared to the Layout; the delay times are less. The Total Chip area of the Layout is 26448.3625 um². It has such a large area because of how we supplied VDD and GND; we made it have a y-size of 20, so it has enough to supply the layout. It was calculated by the size of my chip, which had a width of 145 lambda (25375 nanometer), and a length of 5956 lambda (1042300 nanometer).

Table 8:	Summary	of Measurement	ts
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	LTSPICE	LTSPICE	IRSIM	IRSIM Layout
	Schematic	Layout	Schematic	
Rise Time	Between 0.20 ns - 0.50 ns	Between 0.50 ns - 0.70 ns	Х	X
Fall Time	Between 0.15 ns - 0.40 ns	Between 0.30 ns -0.40 ns	Х	Х
Propagation Delay	Between 0.26 ns - 1.82 ns	Between 0.45 ns - 2.69 ns	Between 0.15 ns - 6.00 ns	Between 0.10 ns -5.50 ns

Table 9: More Measurements

	Schematic	Layout
Transistor Sizes (W/L)	PMOS (10/2), NMOS (5/2)	PMOS (10/2), NMOS (10/2)
Total Chip Area	Х	26448.3625 um ²
Power Dissipation	3.3 V * 0.029 A = 0.0957 Watts	3.3 V * 0.035 A = 0.1155 Watts

Section 10: Comparison of Schematic and Layout:

For LTSPICE, by comparing Figure 10 (Electric Schematic) with Figure 17 (Electric Layout), the way the input and output reacted given the Spice Code appears to be the same. In addition, the inputs and outputs of the computations from Table 4 (Electric Schematic) and Table 6 (Electric Layout) are the same so it verifies our design. The only noticeable difference between the two figures would be the rise time, fall time, and propagation delay, which could be seen on Table 8.

For IRSIM, by comparing Figure 11, 12, 13, 14 (Electric Schematic) with Figure 18, 19, 20, 21 (Electric Layout), respectively, the way the input and output reacted given the certain inputs appears to be the same. In addition, the inputs and outputs of the computations from Table 5 (Electric Schematic) and Table 7 (Electric Layout) are the same so it verifies our design. The only noticeable difference between the figures would be the propagation delay, which could be seen on Table 8.

In conclusion, LTSPICE and IRSIM shows the same form of result towards Electric Schematic and Electric Layout with only a few noticeable differences. The difference that was seen through the figures were the rise time, fall time and propagation delay. The difference can be viewed on Table 8, which has a summary of the measurements.

Section 11: Conclusion:

In this project, we designed a CMOS of a 16-Bit Ripple Carry Adder by connecting 16 Full Adders together. A Full Adder is designed by connecting 2 two input XOR gate and 3 two input NAND gate together. By using the Electric software, we created two different designs, a schematic design and a layout design. We also generated waveforms using two different software, IRSIM and LTSPICE. The two different software helped support our design by increasing our test methods and providing us different test properties. After obtaining the waveforms for the two different design, we compared them and observe their similarities and differences. We observed that for LTSPICE and IRSIM, the input and output reacted the same way given certain inputs for both the Electric Schematic and for the Electric Layout; in addition, it matched the computed values and the goal we were trying to achieve. The only difference between the Electric Schematic and the Electric Layout were the rise time, fall time, and propagation delay. For LTSPICE and IRSIM, these forms of differences can be observed by checking out Table 8, Summary of Measurements. Therefore, based on our observation and the data that was gathered, we can conclude that there isn't a significant difference in terms of the waveforms; however, there is a difference in the rise time, fall time and propagation delay when zooming in on the waveform.

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